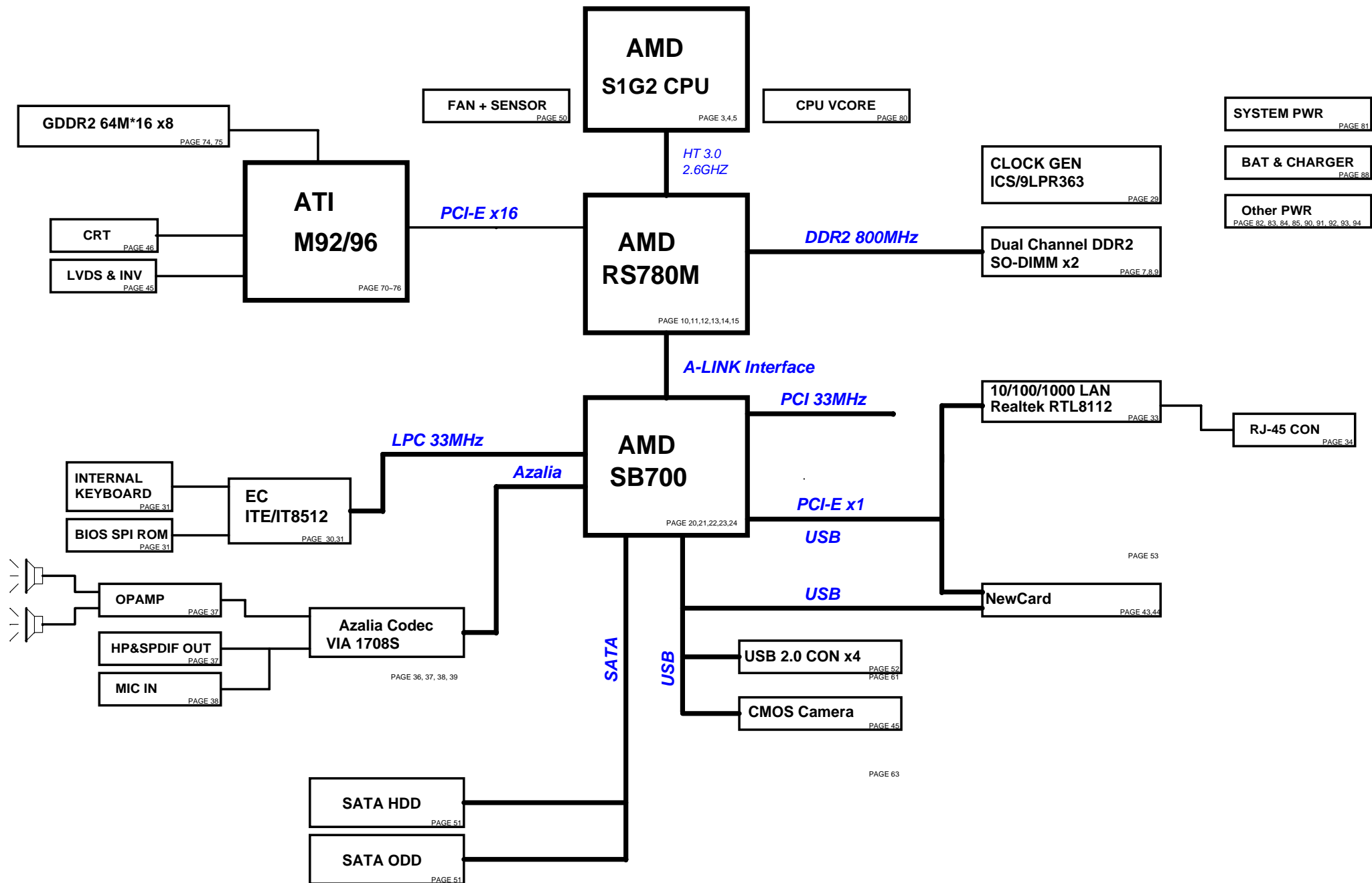
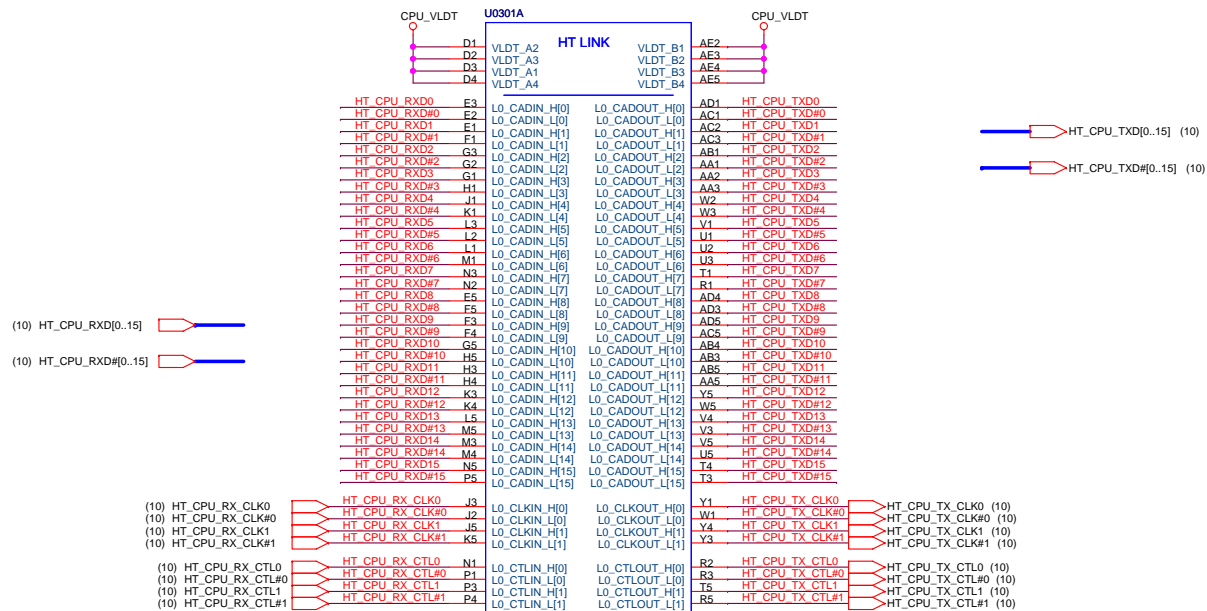


[illegible][illegible]

K40AA Block Diagram



1.5A

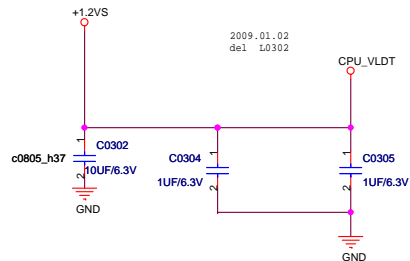


SOCKET638

Change P/N to 12G011306380

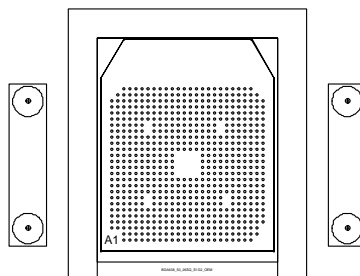
071113

Do not cross plane.

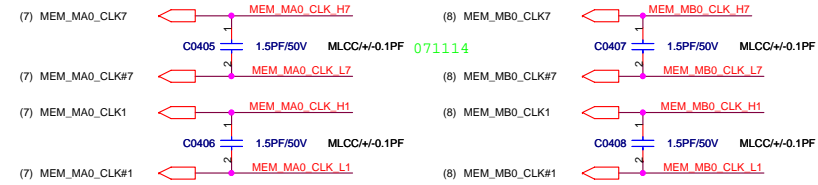


Place close to socket

* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



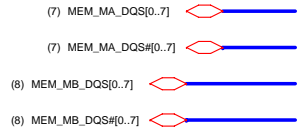
place close to PROCESSOR within 1.5 inch

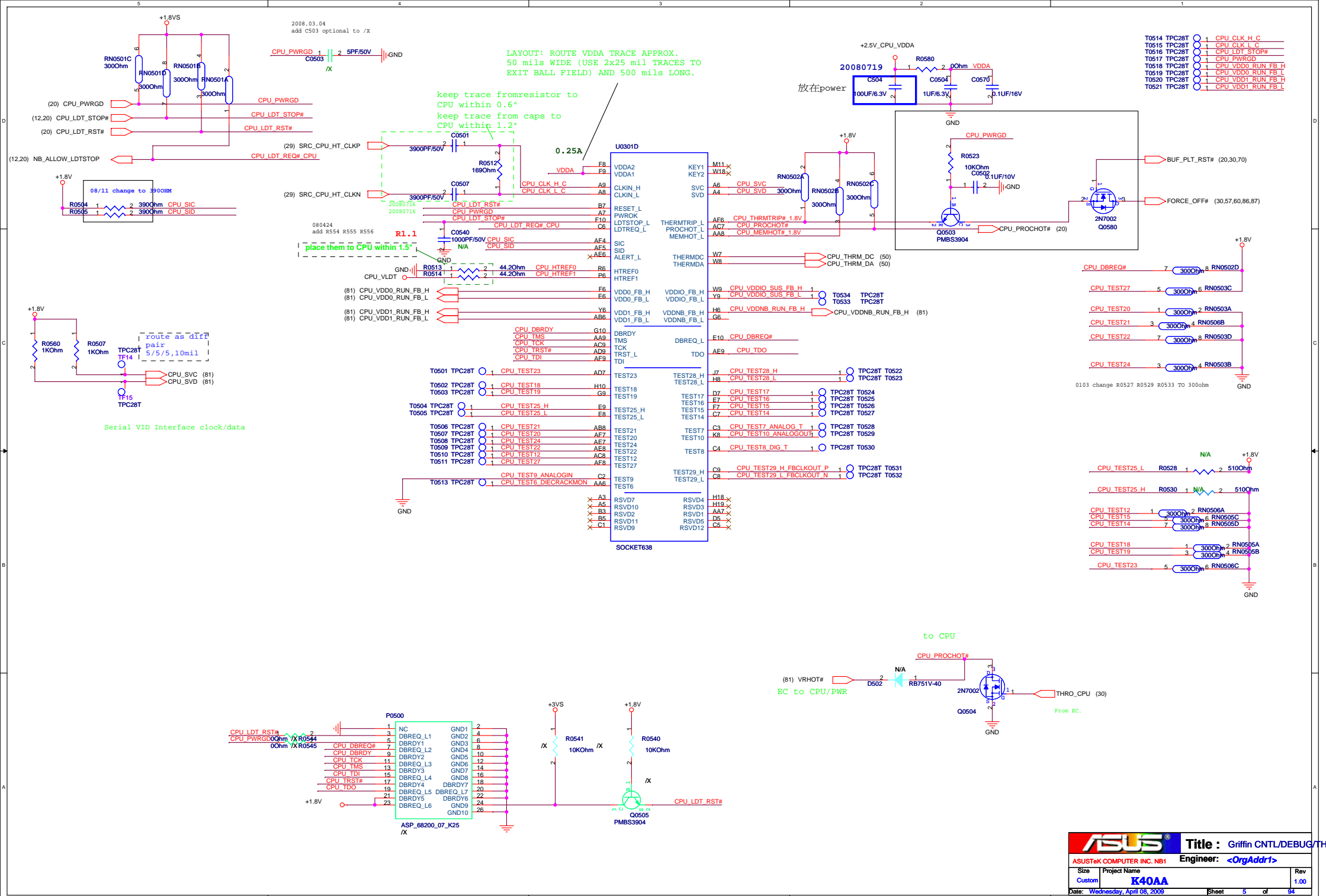


To SODIMM socket 1

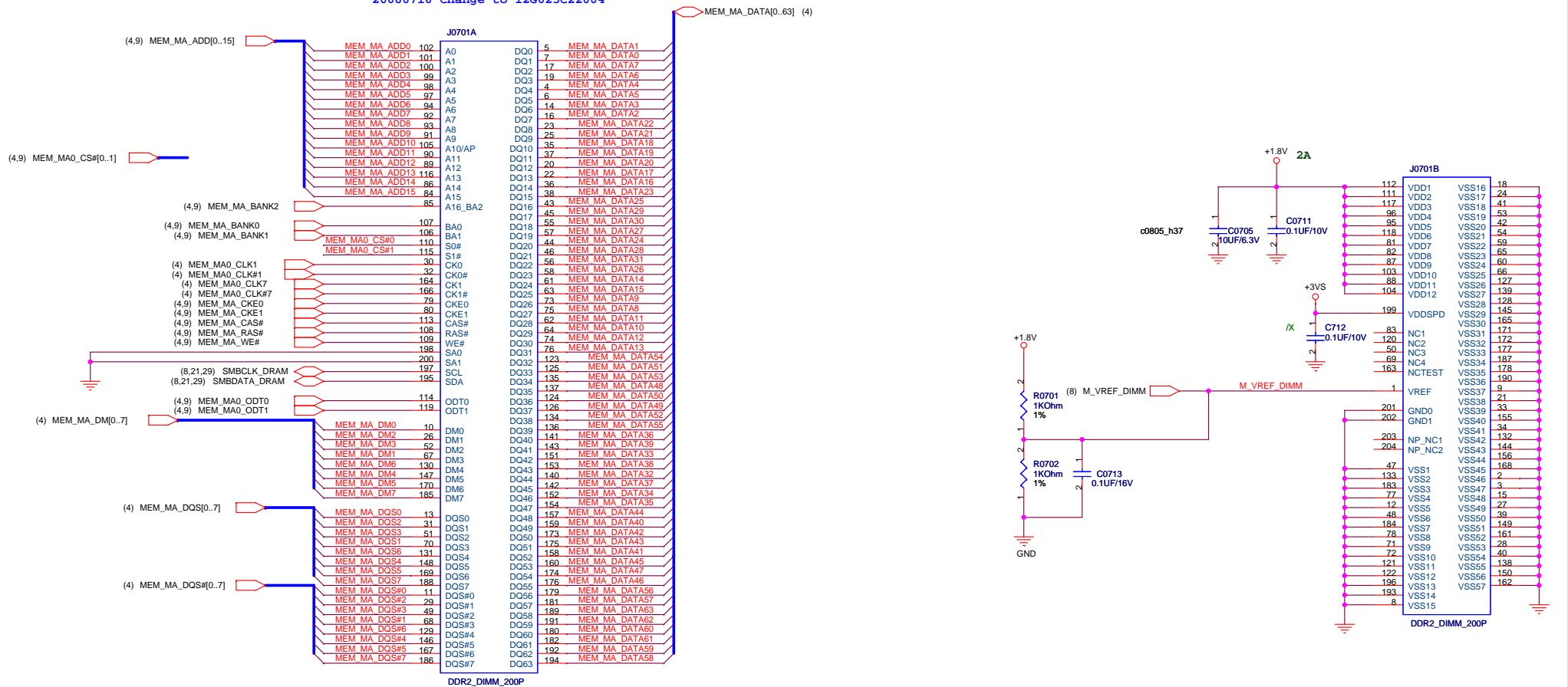


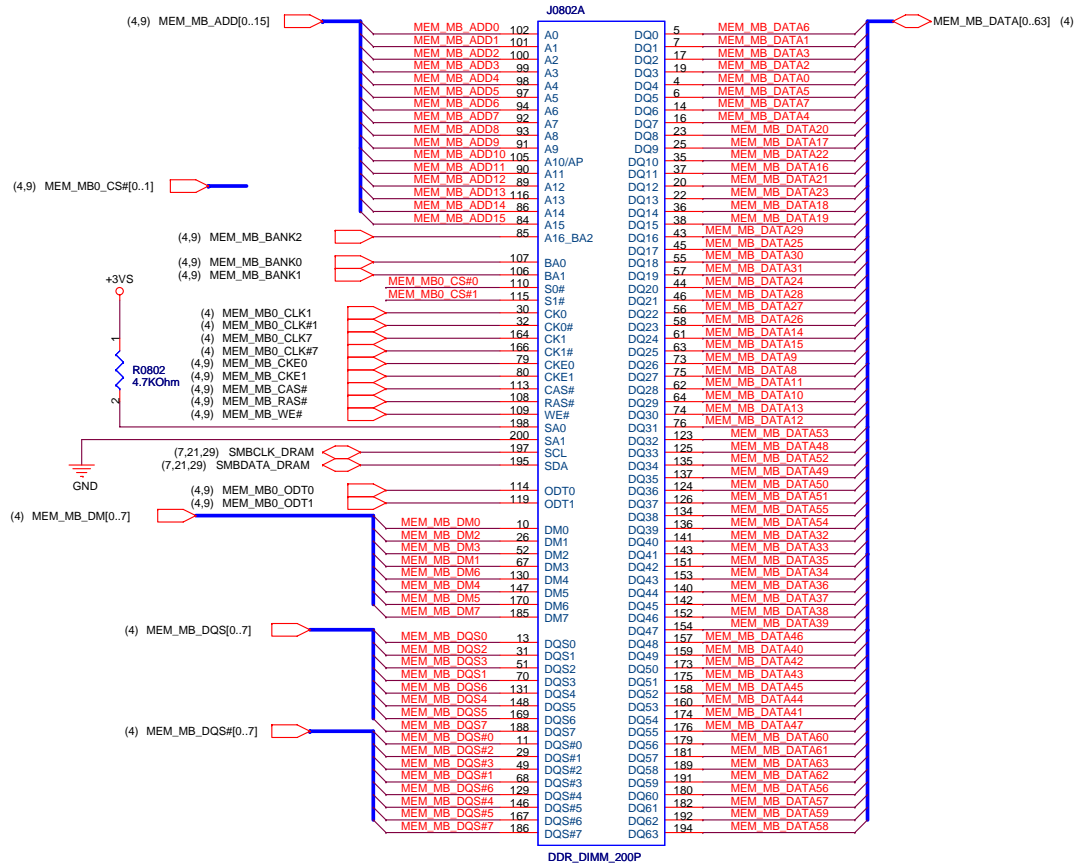
09/23 2.0

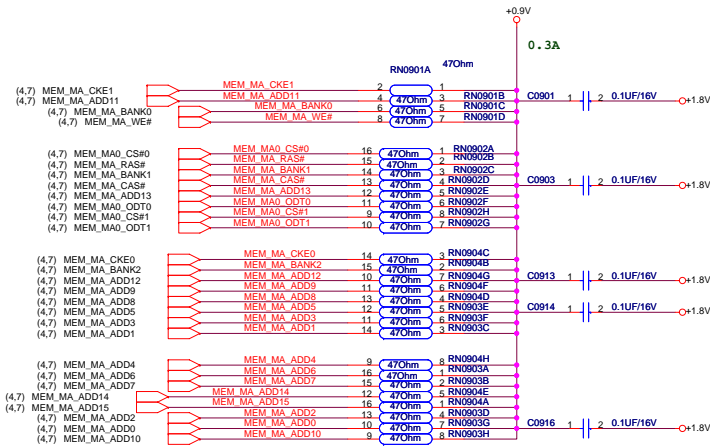




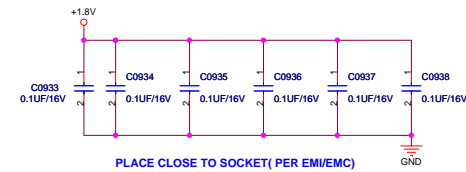
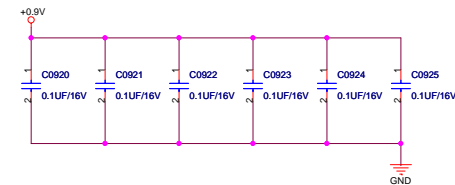
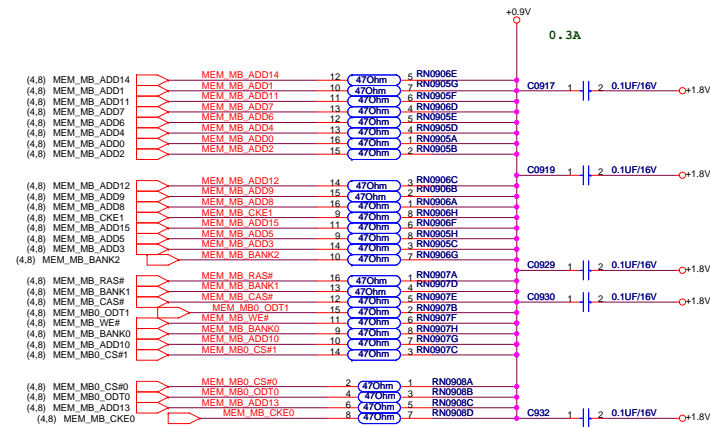
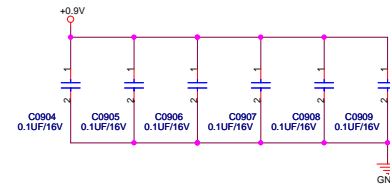
20080716 Change to 12G025C22004

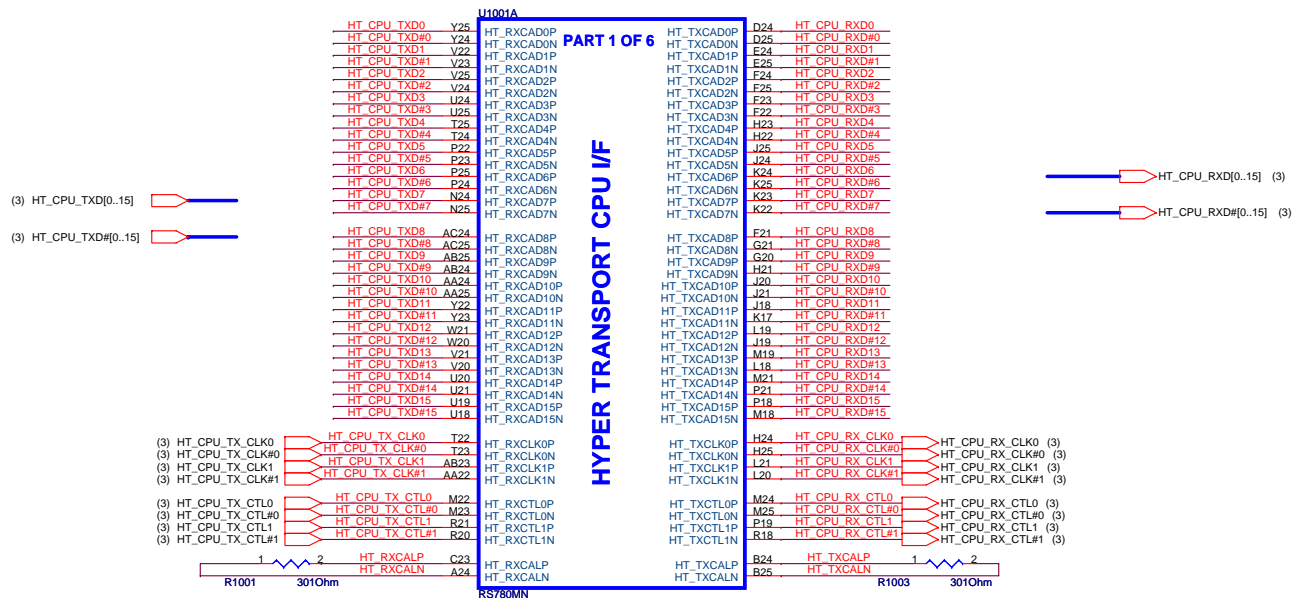






20080803 Remove R907





(70) GFX_VGA_RXP[0..7]
(70) GFX_VGA_RXN[0..7]

PCI-E:
0-3 HDMI@ RS780M
4~7 NC
8-15 VGA8x

U1001B

PART 2 OF 6

PCI-E I/F GFX

GFX_VGA_RXP7
GFX_VGA_RXN7
GFX_VGA_RXP6
GFX_VGA_RXN6
GFX_VGA_RXP5
GFX_VGA_RXN5
GFX_VGA_RXP4
GFX_VGA_RXN4
GFX_VGA_RXP3
GFX_VGA_RXN3
GFX_VGA_RXP2
GFX_VGA_RXN2
GFX_VGA_RXP1
GFX_VGA_RXN1
GFX_VGA_RXP0
GFX_VGA_RXN0

AE3
AD4
AE2
AD3
AD1
AD2
V5
V6
U5
U6
U8
U7

PCI-E I/F GPP

(33) PCIE_RXP1_LAN
(33) PCIE_RXN1_LAN
(53) PCIE_RXP2_WLAN
(53) PCIE_RXN2_WLAN

PCI-E I/F SB

(20) PCIE_SB_NB_RX0P
(20) PCIE_SB_NB_RX0N
(20) PCIE_SB_NB_RX1P
(20) PCIE_SB_NB_RX1N
(20) PCIE_SB_NB_RX2P
(20) PCIE_SB_NB_RX2N
(20) PCIE_SB_NB_RX3P
(20) PCIE_SB_NB_RX3N

AA8
Y8
AA7
Y7
AA6
Y6
W5
Y5

RS780MN

GFX_TX0P
GFX_TX0N
GFX_TX1P
GFX_TX1N
GFX_TX2P
GFX_TX2N
GFX_TX3P
GFX_TX3N
GFX_TX4P
GFX_TX4N
GFX_TX5P
GFX_TX5N
GFX_TX6P
GFX_TX6N
GFX_TX7P
GFX_TX7N
GFX_TX8P
GFX_TX8N
GFX_TX9P
GFX_TX9N
GFX_TX10P
GFX_TX10N
GFX_TX11P
GFX_TX11N
GFX_TX12P
GFX_TX12N
GFX_TX13P
GFX_TX13N
GFX_TX14P
GFX_TX14N
GFX_TX15P
GFX_TX15N

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_TX4P
GPP_TX4N
GPP_TX5P
GPP_TX5N

SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N

PCE_CALRP
PCE_CALRN

AC8
AB8

1.27KOHM
2KOHM

R1101
R1102

+1.1V_NB
GND

AC1
AC2
AB4
AB3
AA2
AA1
Y1
Y2
Y3
Y4
V1
V2
AD7
AE7
AE6
AD6
AB6
AC6
AD5
AE5
C1107
C1109
C1108
C1110
C1111
C1112
C1114
C1116

1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V
2 1 0.1UF/10V

PCIE_TXP1_LAN C
PCIE_TXN1_LAN C
PCIE_TXP2_WLAN C
PCIE_TXN2_WLAN C
A_TX0P C
A_TX0N C
A_TX1P C
A_TX1N C
A_TX2P C
A_TX2N C
A_TX3P C
A_TX3N C

PCIE_TXP1_LAN (33)
PCIE_TXN1_LAN (33)
PCIE_TXP2_WLAN (53)
PCIE_TXN2_WLAN (53)
PCIE_NB_SB_TX0P (20)
PCIE_NB_SB_TX0N (20)
PCIE_NB_SB_TX1P (20)
PCIE_NB_SB_TX1N (20)
PCIE_NB_SB_TX2P (20)
PCIE_NB_SB_TX2N (20)
PCIE_NB_SB_TX3P (20)
PCIE_NB_SB_TX3N (20)

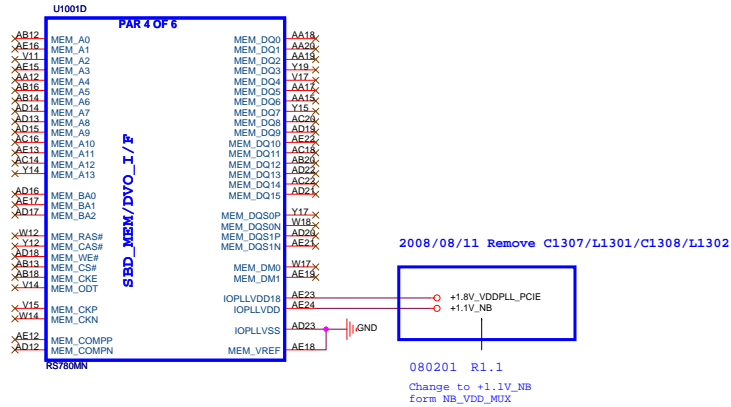
PCIENB_TXN0 C1142 2 1 0.1UF/10V GFX_VGA_TXN0
PCIENB_TXN1 C1144 2 1 0.1UF/10V GFX_VGA_TXN1
PCIENB_TXN2 C1141 2 1 0.1UF/10V GFX_VGA_TXN2
PCIENB_TXN3 C1148 2 1 0.1UF/10V GFX_VGA_TXN3
PCIENB_TXN4 C1145 2 1 0.1UF/10V GFX_VGA_TXN4
PCIENB_TXN5 C1147 2 1 0.1UF/10V GFX_VGA_TXN5
PCIENB_TXN6 C1143 2 1 0.1UF/10V GFX_VGA_TXN6
PCIENB_TXN7 C1146 2 1 0.1UF/10V GFX_VGA_TXN7

(70) GFX_VGA_TXN[0..7]

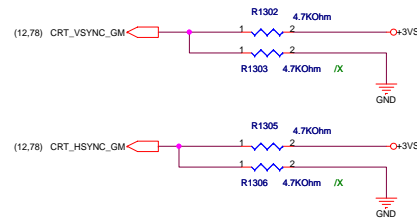
PCIENB_TXP0 C1149 2 1 0.1UF/10V GFX_VGA_TXP0
PCIENB_TXP1 C1150 2 1 0.1UF/10V GFX_VGA_TXP1
PCIENB_TXP2 C1151 2 1 0.1UF/10V GFX_VGA_TXP2
PCIENB_TXP3 C1156 2 1 0.1UF/10V GFX_VGA_TXP3
PCIENB_TXP4 C1152 2 1 0.1UF/10V GFX_VGA_TXP4
PCIENB_TXP5 C1155 2 1 0.1UF/10V GFX_VGA_TXP5
PCIENB_TXP6 C1153 2 1 0.1UF/10V GFX_VGA_TXP6
PCIENB_TXP7 C1154 2 1 0.1UF/10V GFX_VGA_TXP7

(70) GFX_VGA_TXP[0..7]

R1.11 080319
Change the NB Part number to RS780 (A13)



080118
Disable Side Port Memory
R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

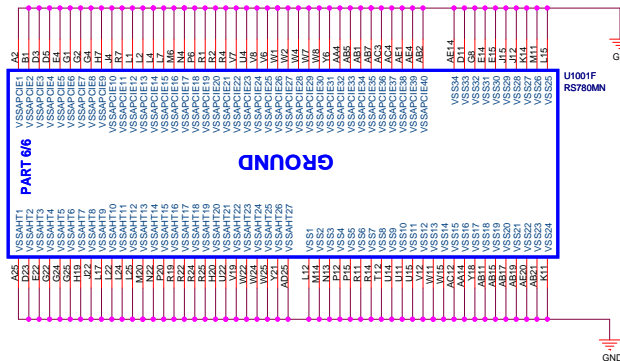
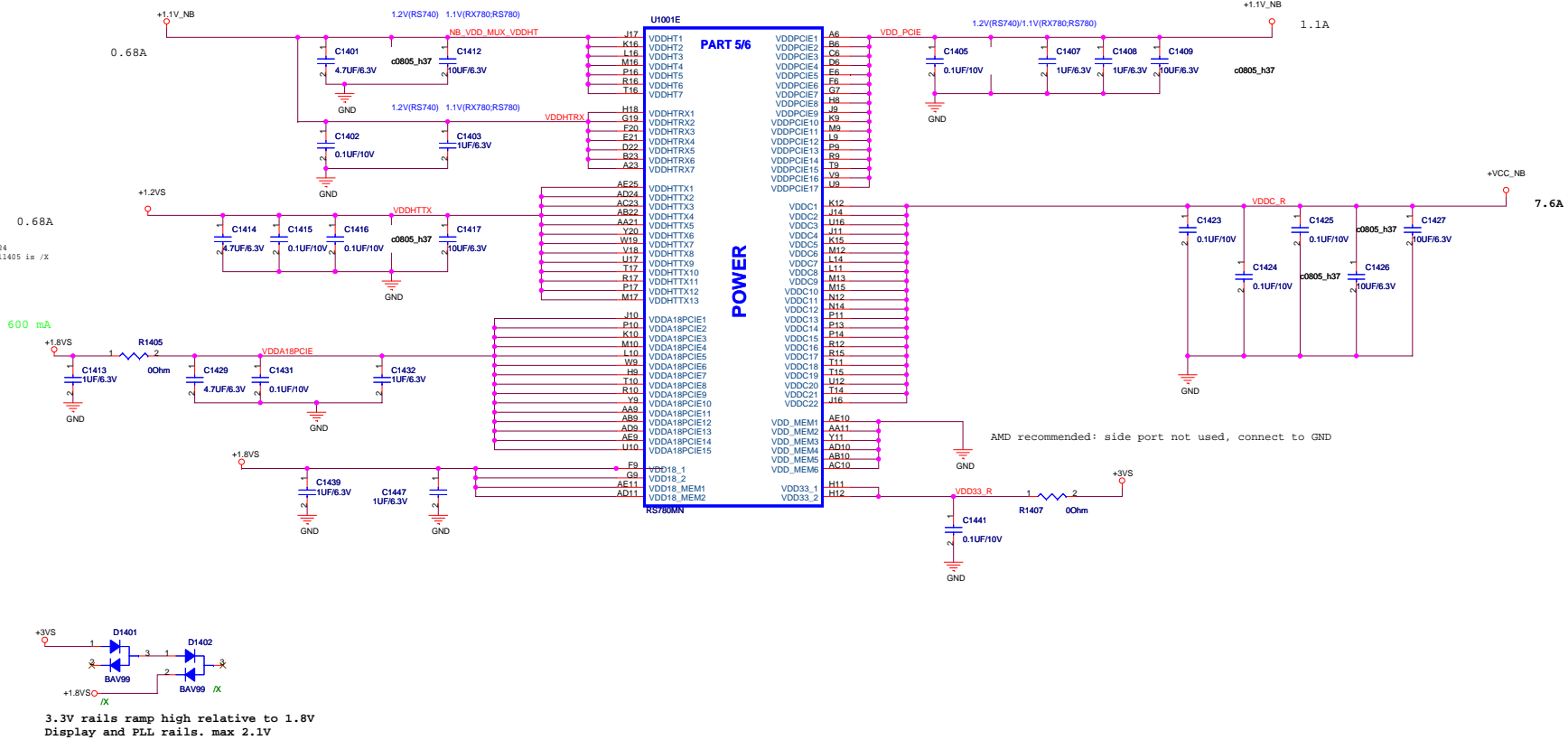
RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory


RS780:HSYNCH

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



5	4	3	2	1						
D				D						
C				C						
B				B						
A				A						
<div><div><div>ASUS®</div><div>ASUSTeK COMPUTER INC. NB1</div><div><table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>K40AA</td><td>1.00</td></tr></table></div></div><div><div>Title :</div><div>Engineer: <OrgAddr1></div><div><div>Date: Wednesday, April 08, 2009</div><div>Sheet 15 of 94</div></div></div></div>					Size	Project Name	Rev	A	K40AA	1.00
Size	Project Name	Rev								
A	K40AA	1.00								
5	4	3	2	1						

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 16 of 94	



Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

Size
A


Project Name

K40AA


Rev
1.00

Date: Wednesday, April 08, 2009

Sheet 17 of 94

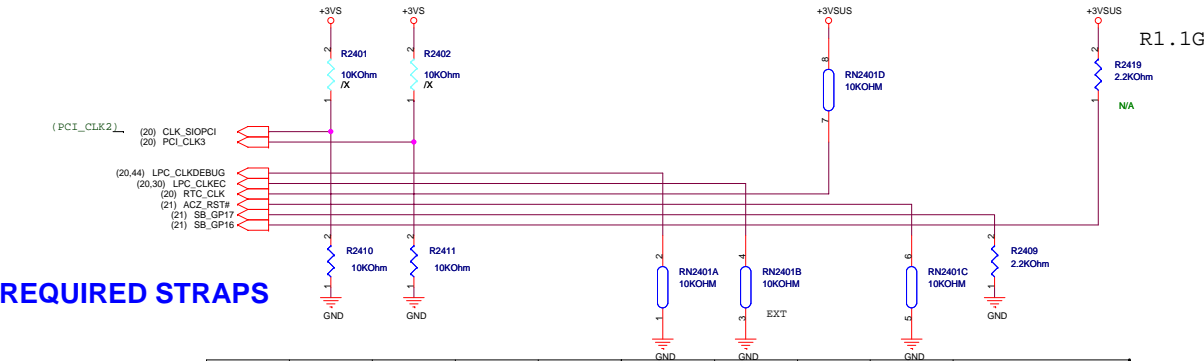
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 18 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet	19 of 94




NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

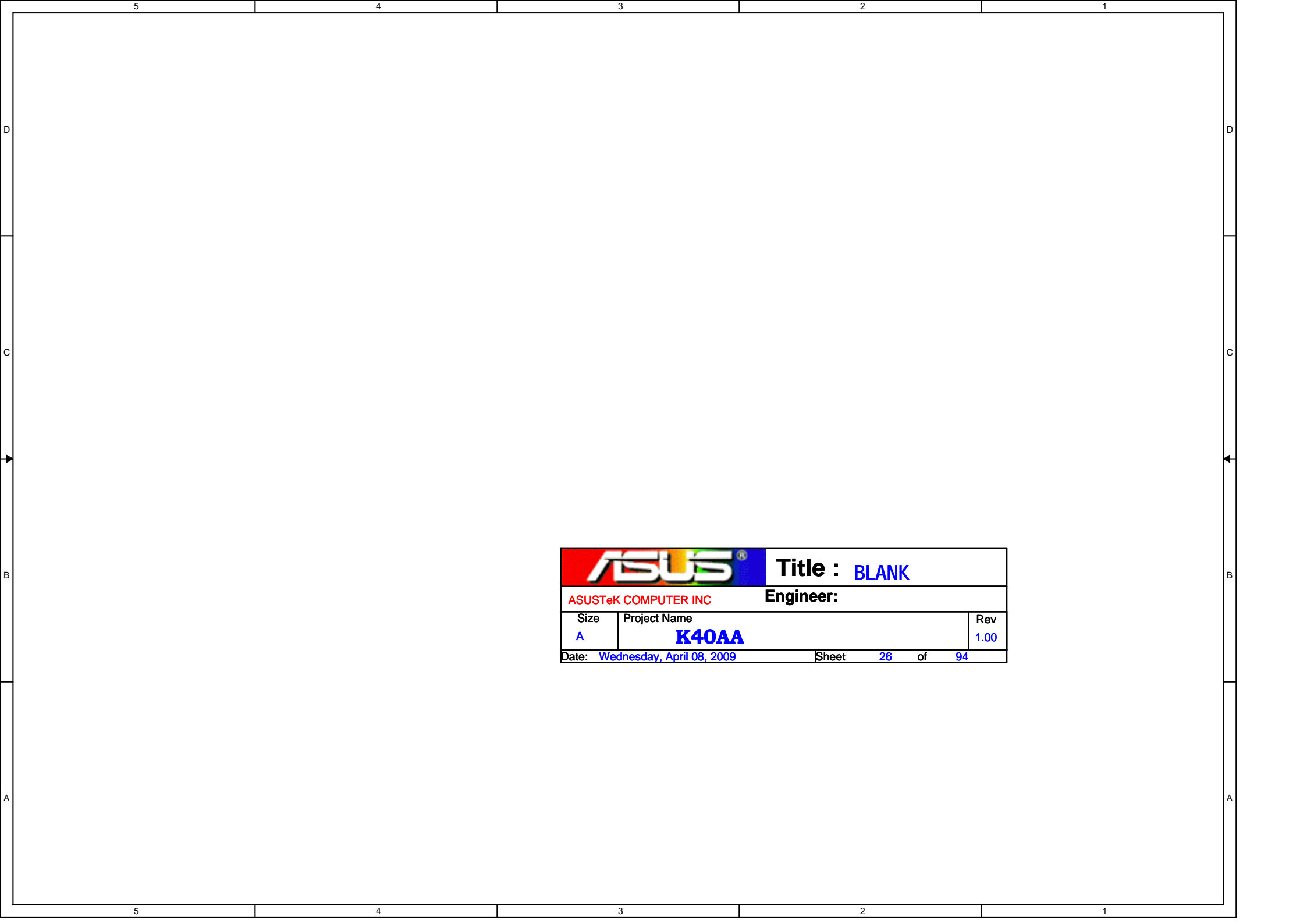



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	32-kHz clock ENABLED	INTERNAL RTC DEFAULT	Integrated Microcontroller ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	32-kHz clock DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	Integrated Microcontroller DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.


5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	K40AA		1.00
Date: Wednesday, April 08, 2009		Sheet 25 of 94	




		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 26 of 94	

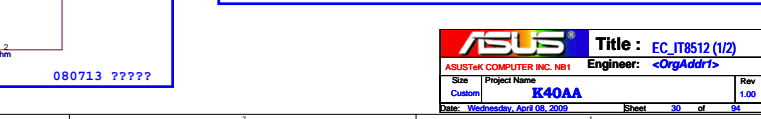
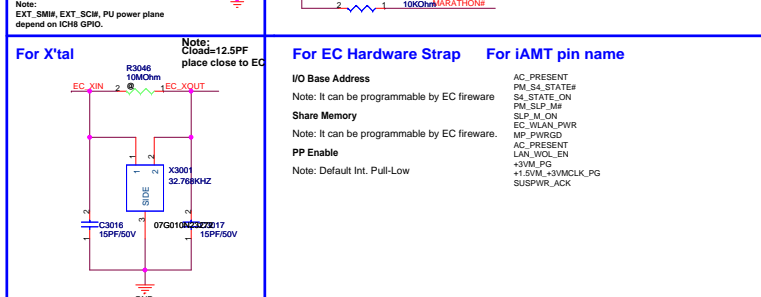
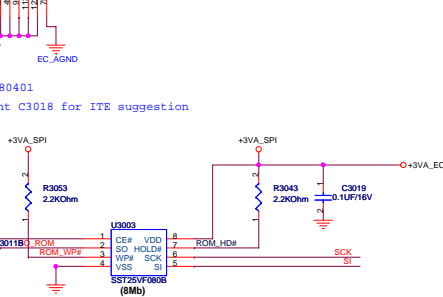
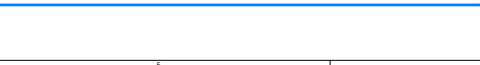
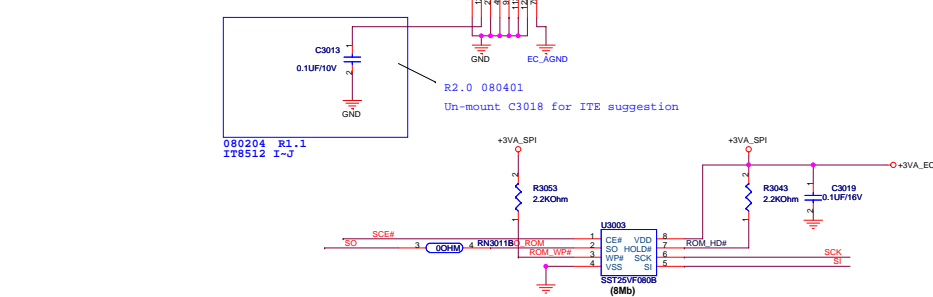
5	4	3	2	1
D				D
C				C
B				B
A				A

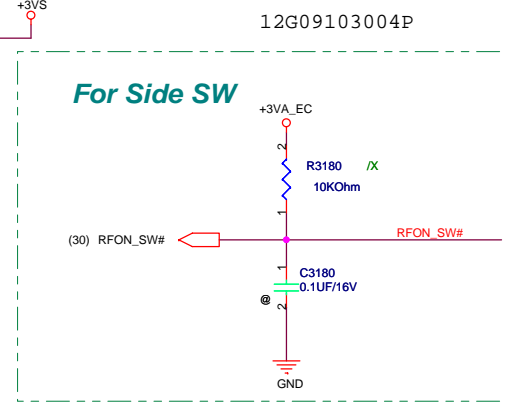
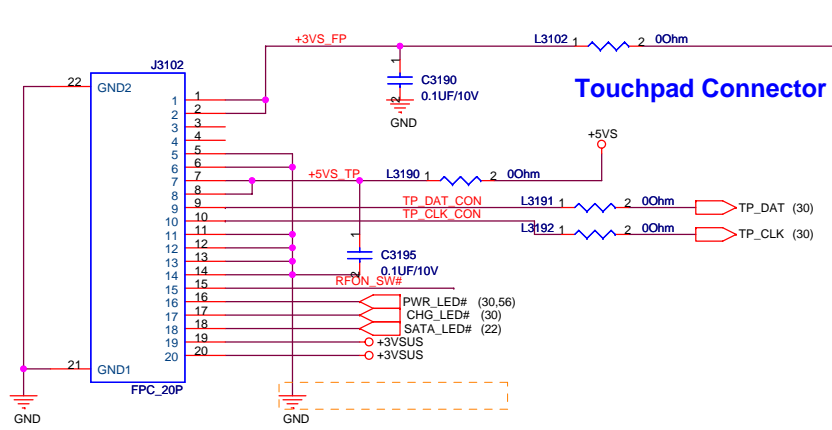
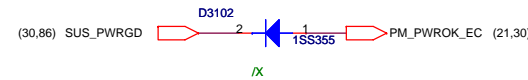
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	K40AA		1.00
Date: Wednesday, April 08, 2009		Sheet 27 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 28 of 94	

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

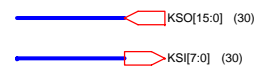




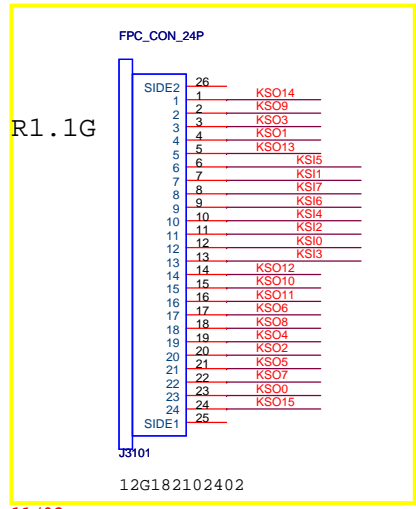
close to connector

Note:
LID_SW# is easy to cause high voltage damage when
plugging inverter board connector to M/B with AC present.
Need to add bidirectional diode to protect this pin.

Keyboard Connector

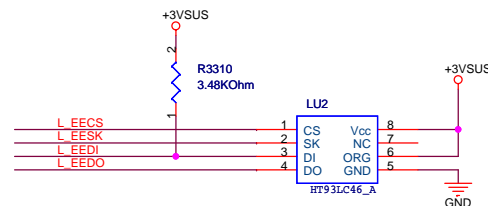
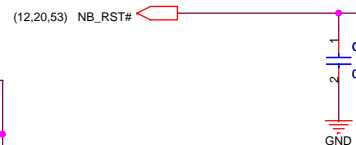
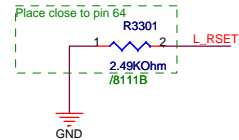
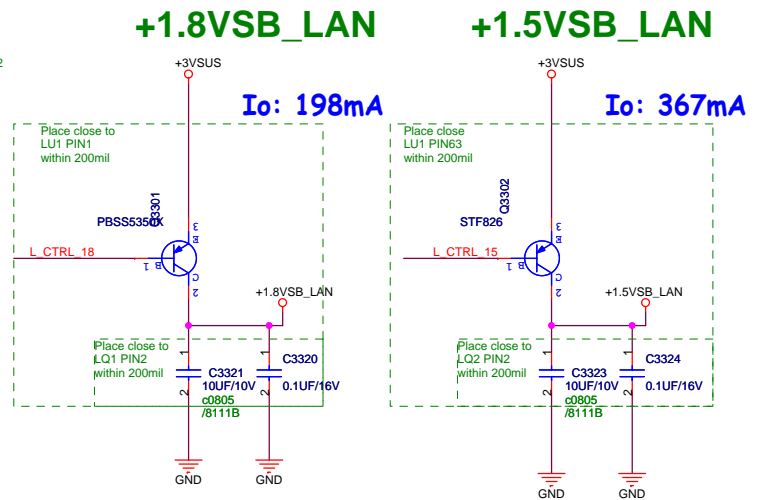


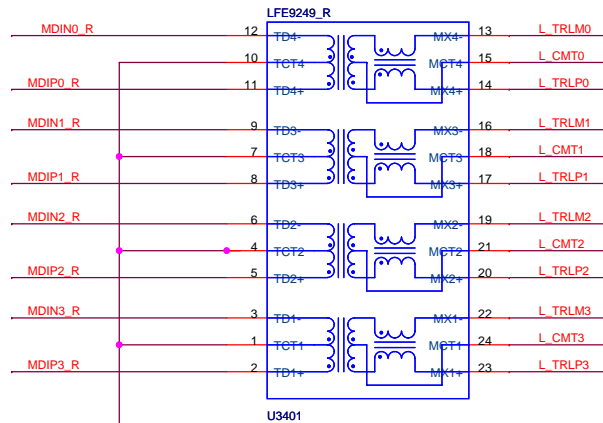
F7/N1 Keyboard



11 / 02

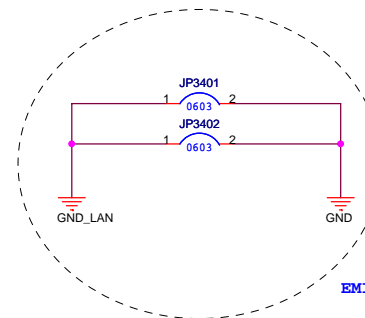
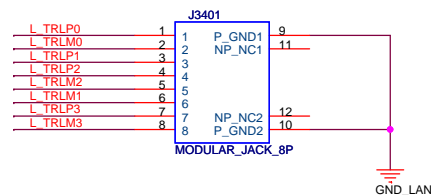
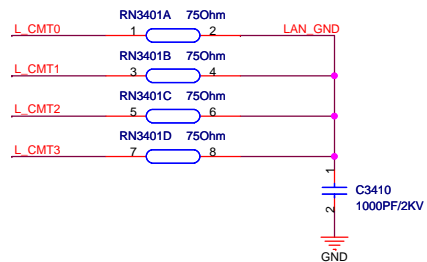
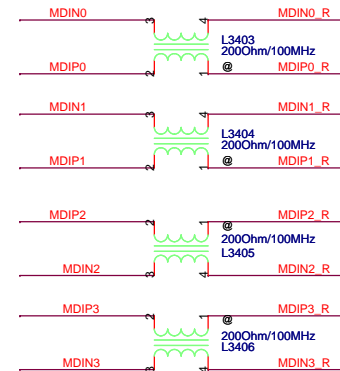
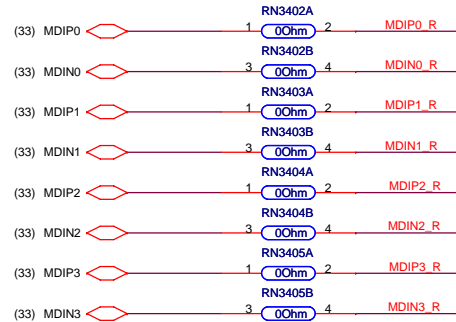






R1.1

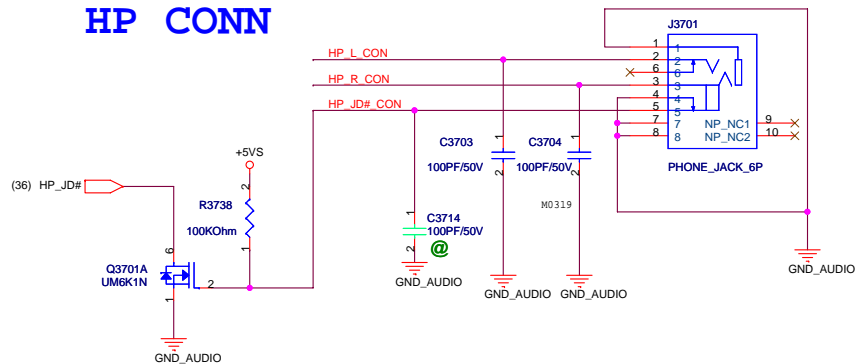
Colay FOR EMI



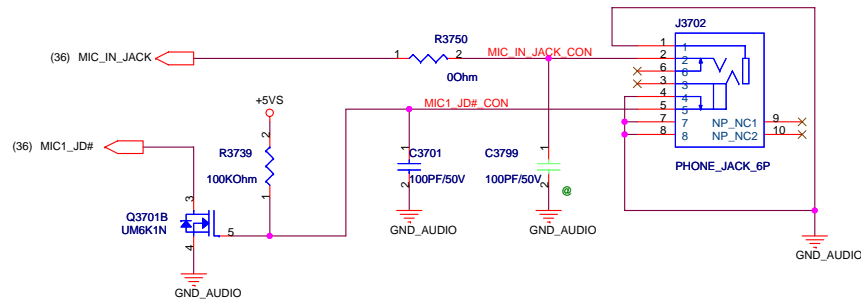
EMI



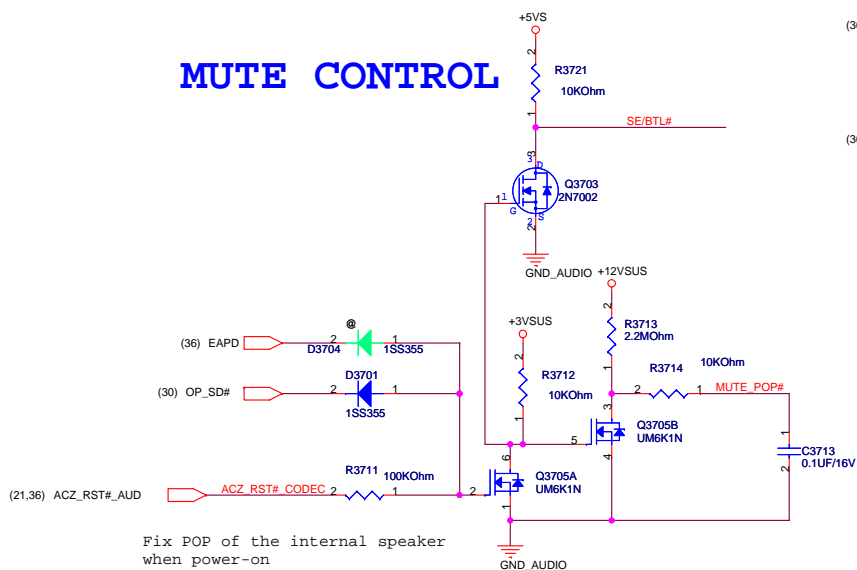
HP CONN



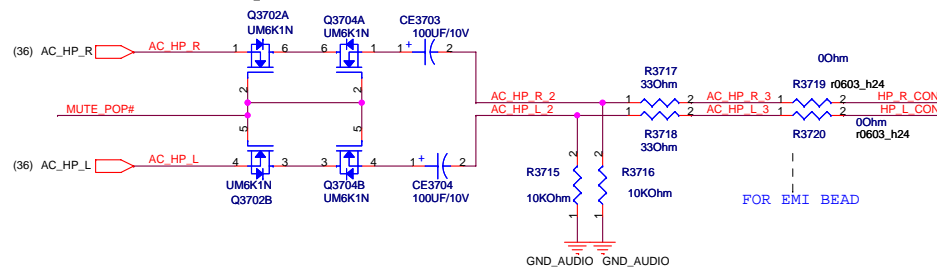
External MIC CONN



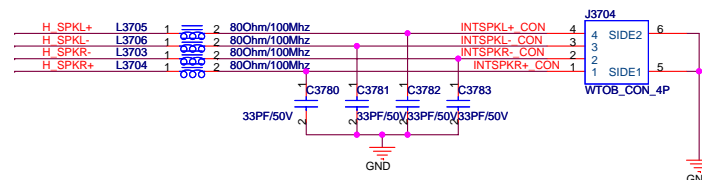
MUTE CONTROL



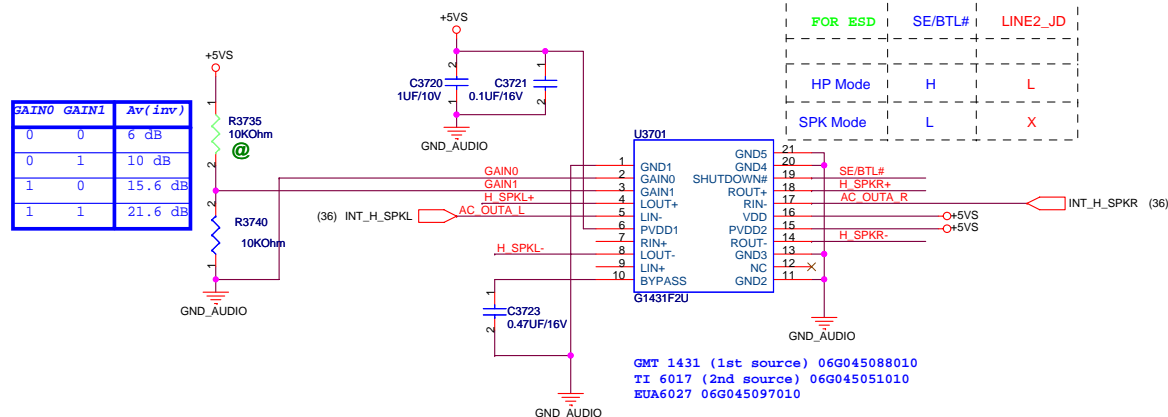
Fix POP of the internal speaker when power-on



SPEAKER CONNECTOR (2W)

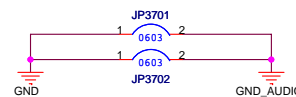


SPEAKER AMP




GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB


	FOR ESD	SE/BTL#	LINE2_JD
HP Mode		H	L
SPK Mode		L	X





		Title : MIC&LINEIN	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	K40AA		1.00
Date: Wednesday, April 08, 2009		Sheet	38 of 94

	5	4	3	2	1
D					D
C					C
B					B
A					A

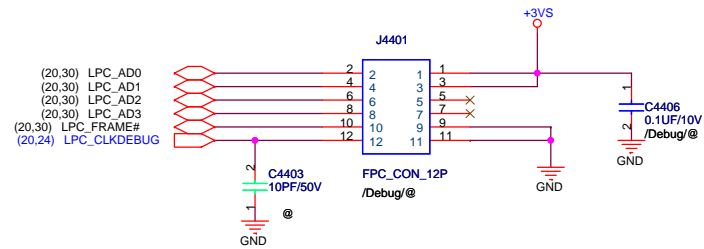
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 39 of 94	











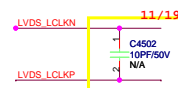
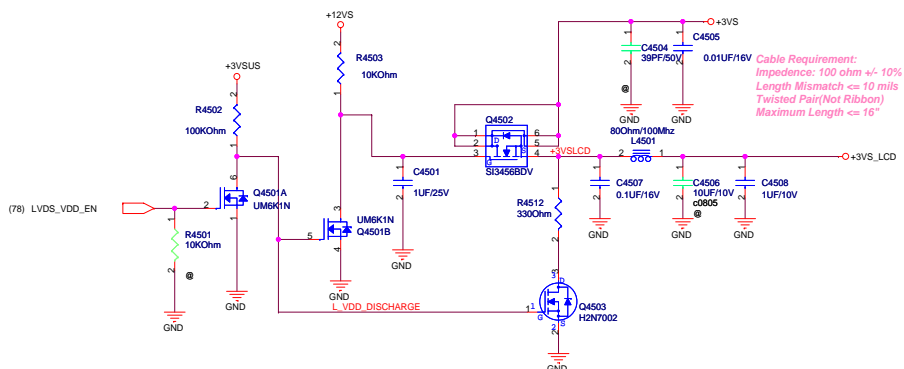
If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

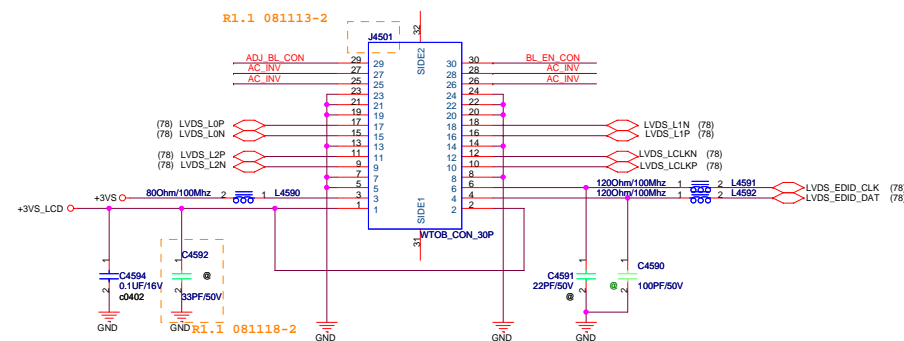
LCD Backlight Control

LCD Power

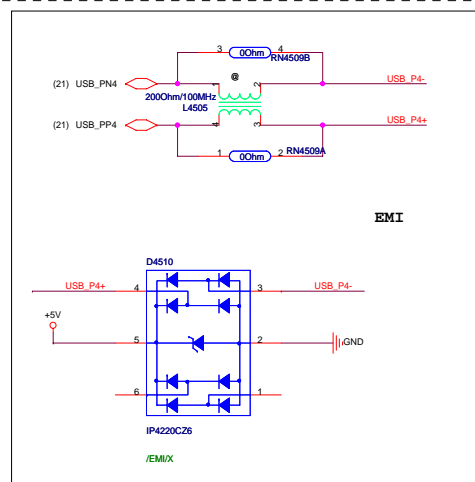
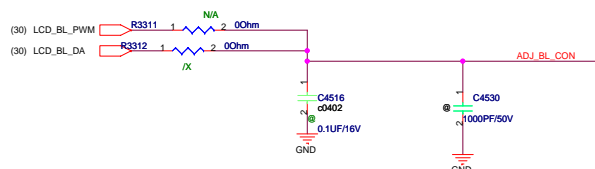
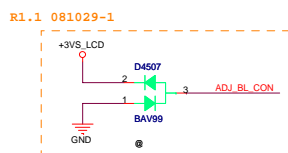


LED PANEL LVDS Interface

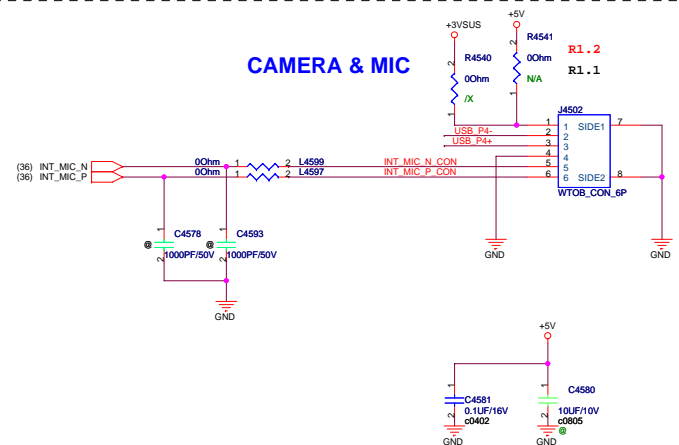
check



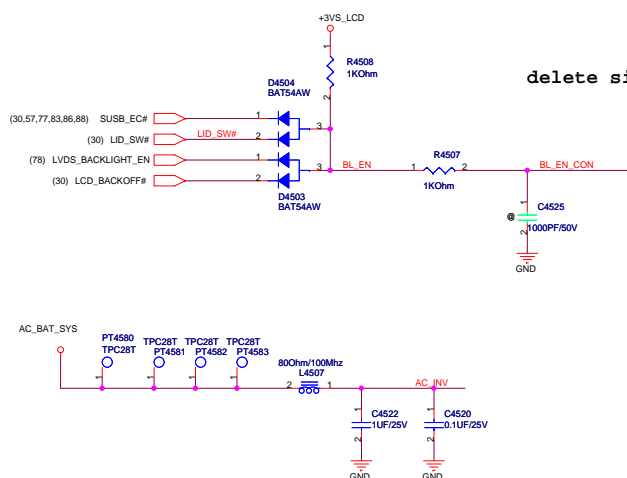
INVERTER
Interface/Speaker CONN.



CAMERA & MIC

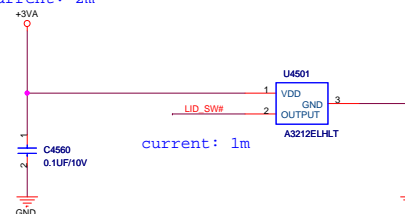


delete sim card function 20080804

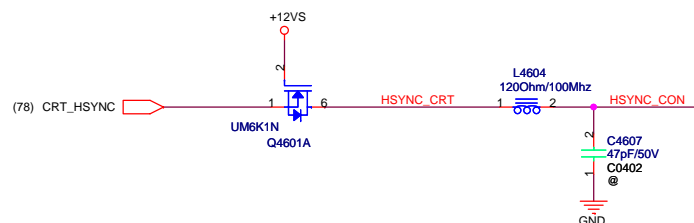
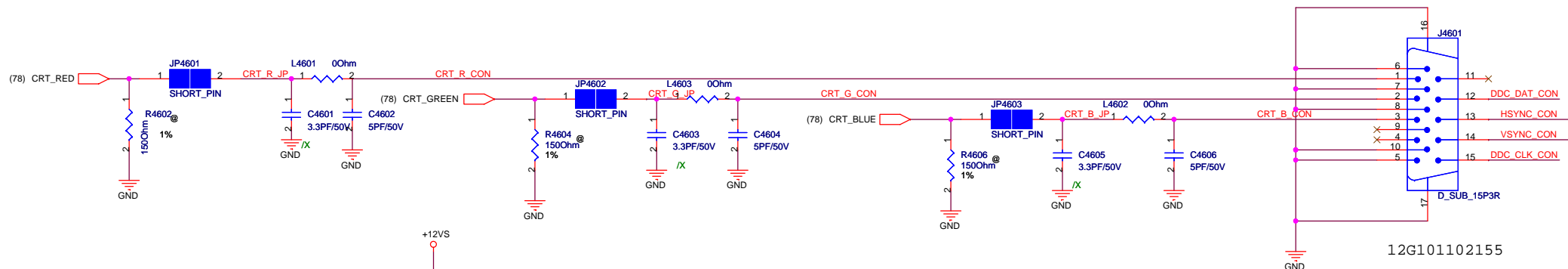


Hall effect switch

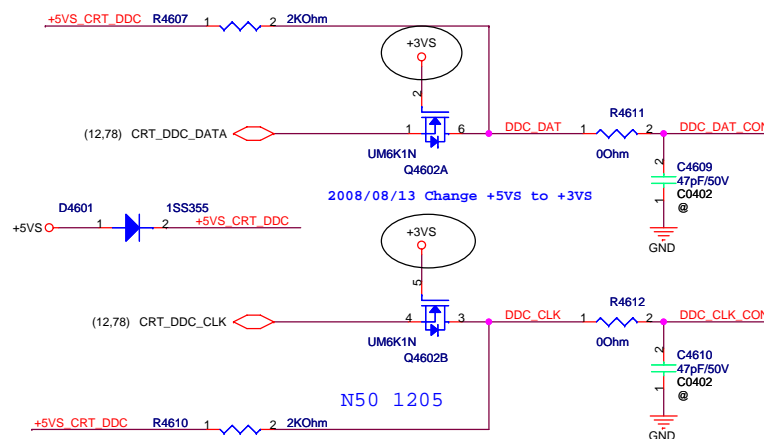
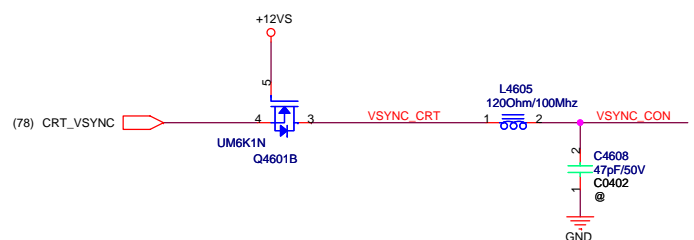
```
current: 2m
```



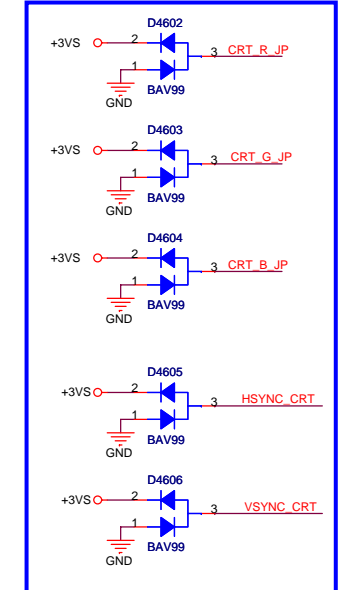
R1.1 VGA部分調整：L4601、L4602、L4603調成0 ohm，C4601、C4603、C4605改爲"/X"，C4602、C4604、C4606改成5PF。




2008/0807 Remove U4601/U4602



PLACE ESD Diodes near VGA port



	5	4	3	2	1
D					
C					
B					
A					



Title : BLANK

ASUSTeK COMPUTER INC

Engineer:


Size	Project Name	Rev
A	K40AA	1.00

Date: Wednesday, April 08, 2009

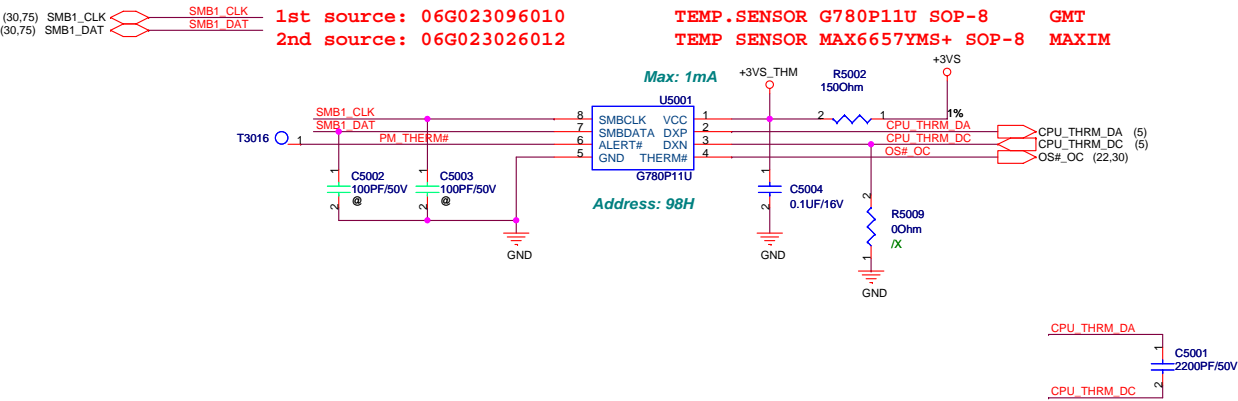
Sheet 47 of 94



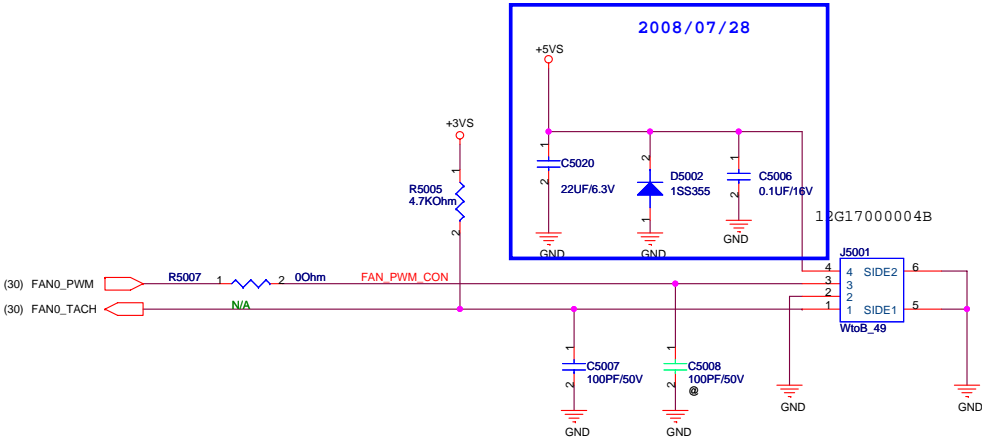
	5	4	3	2	1
D					D
C					C
B					B
A					A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 49 of 94	

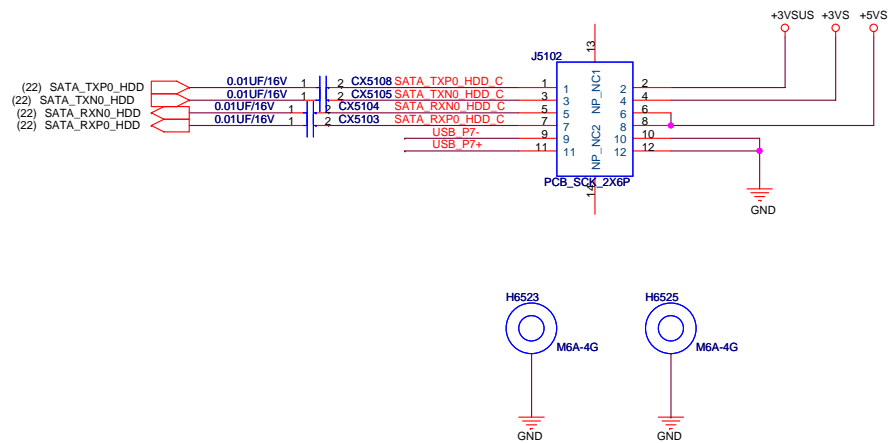
Thermal Sensor



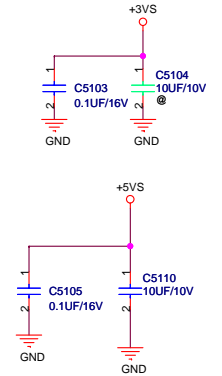
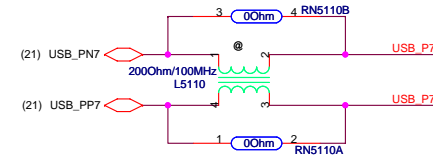
DC FAN Control



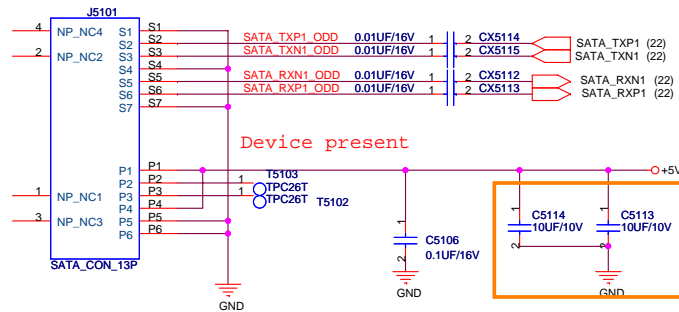
SATA HDD



USB Cardreader

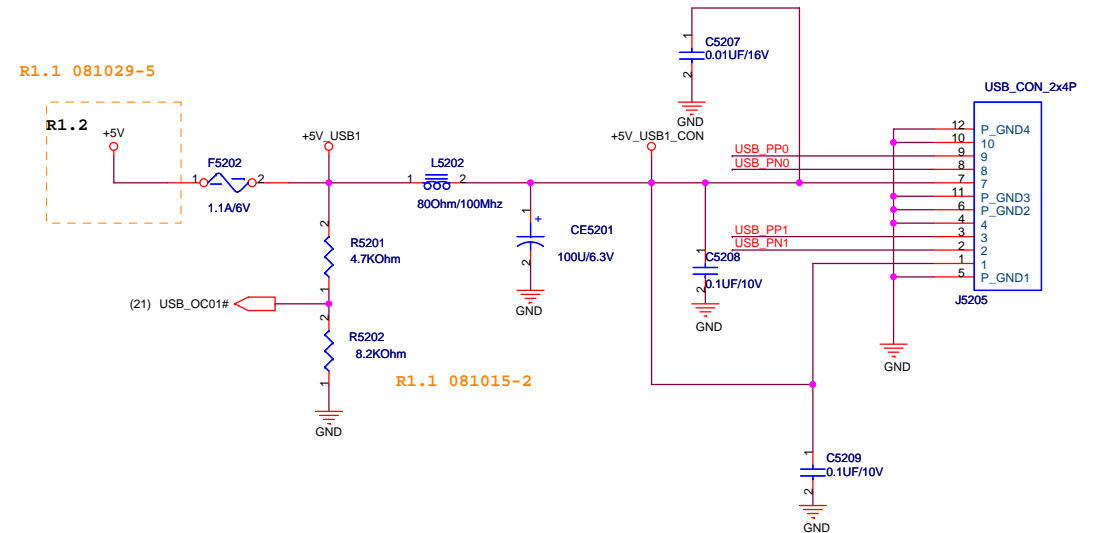
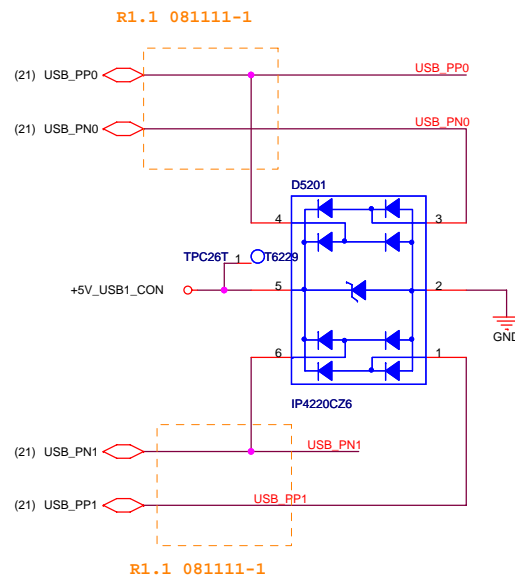
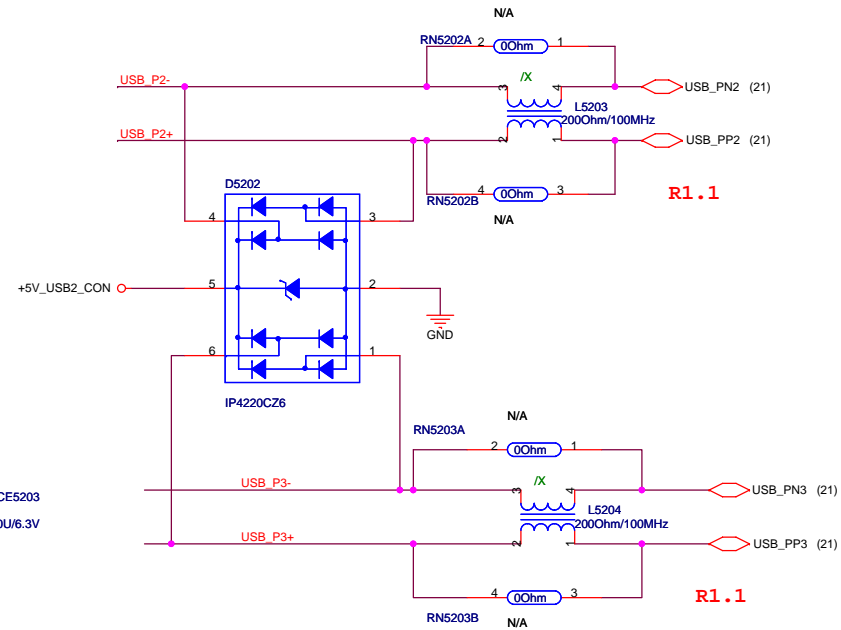
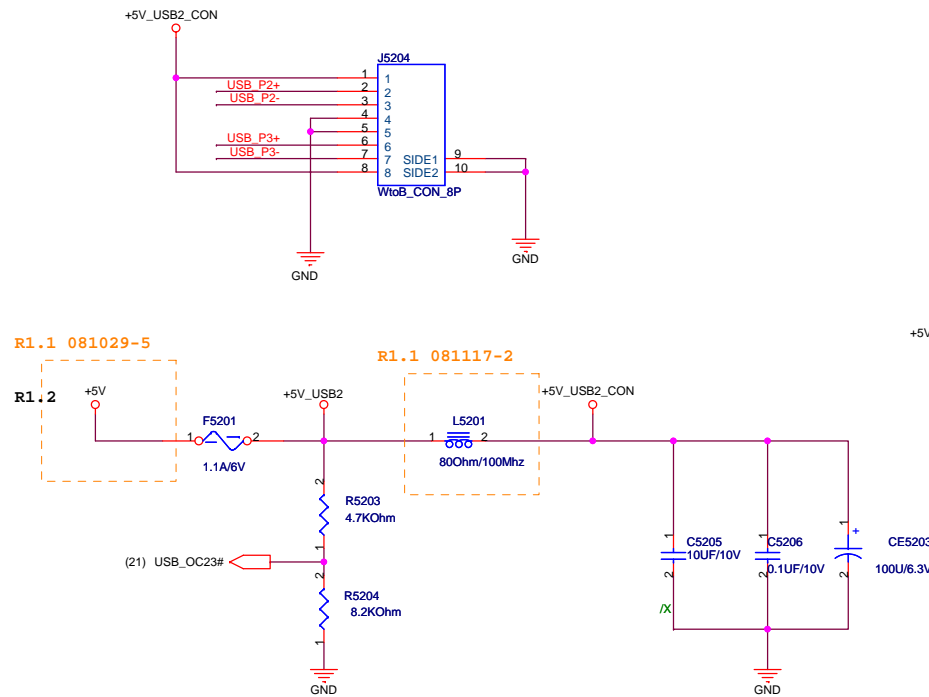


ODD

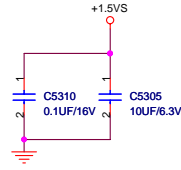
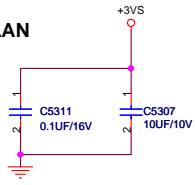


R2.0 06/11

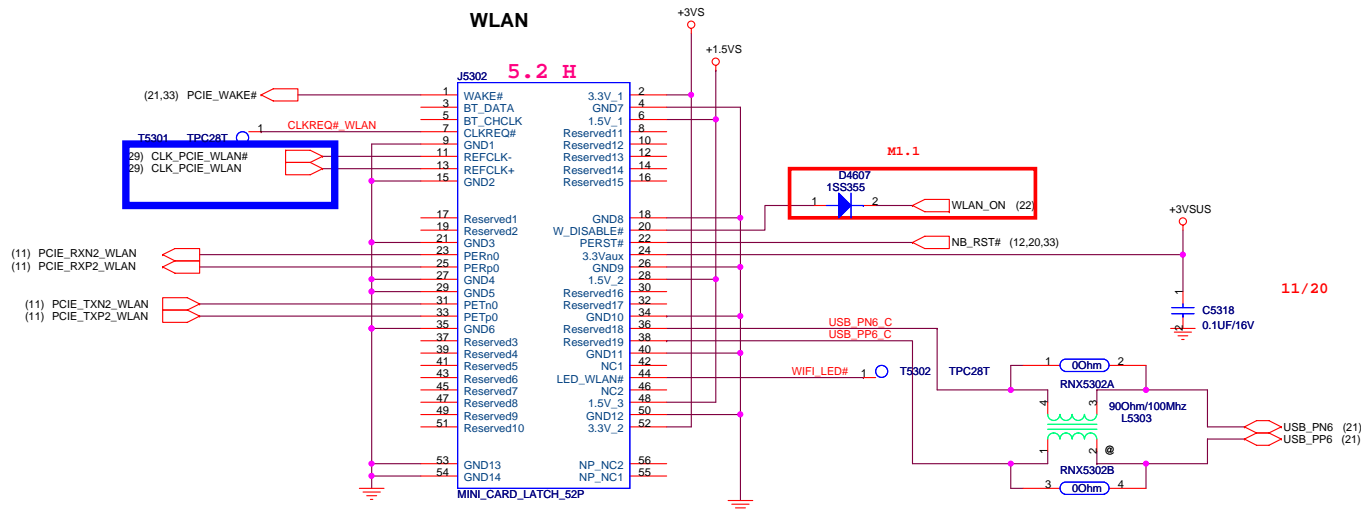
USB IO Board




WLAN




WLAN



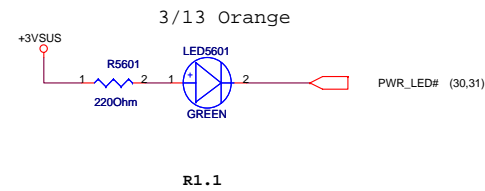
5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet	54 of 94

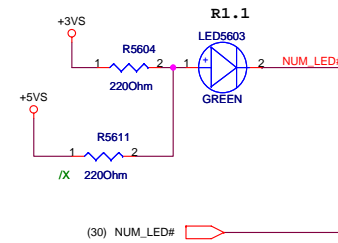
	A	B	C	D	E
1					
2					
3					
4					
5					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Wednesday, April 08, 2009		Sheet 55 of 94	

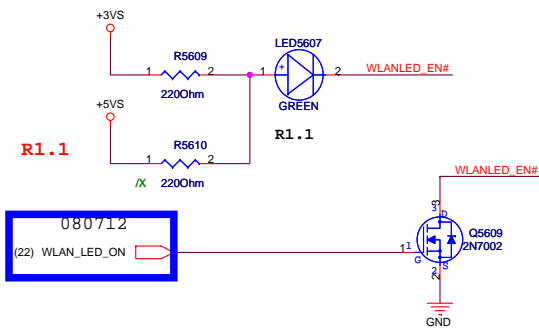
For Power LED



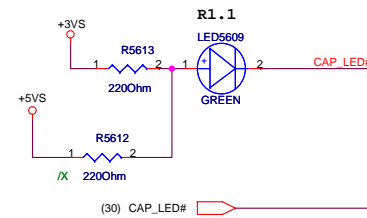
For Number Lock



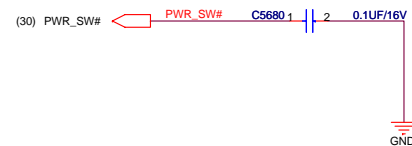
For WireLess LED



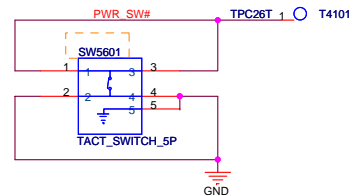
For Caps. Lock

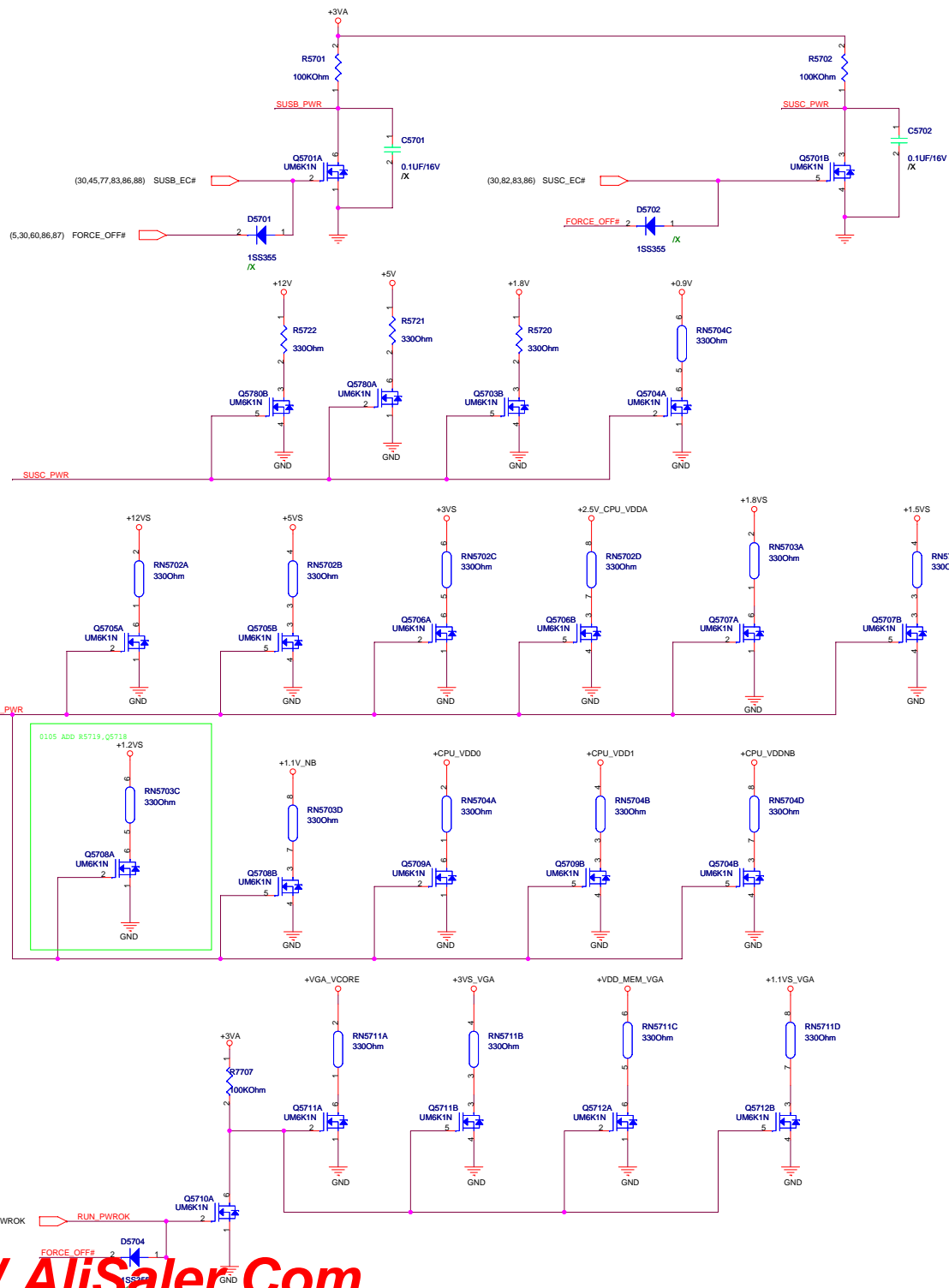


SW



SHUT_DOWN#

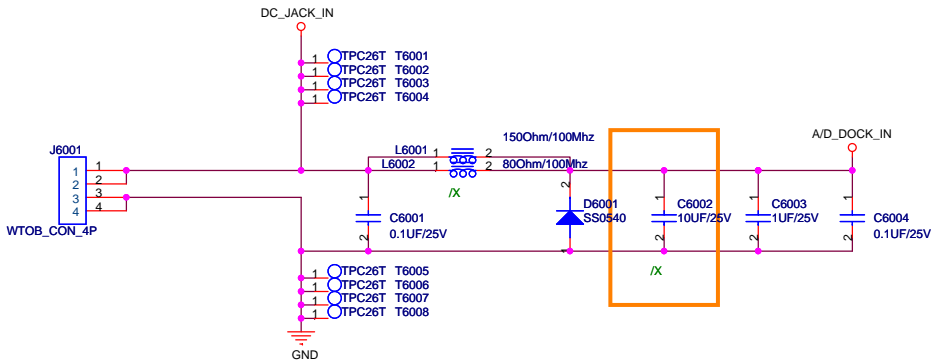




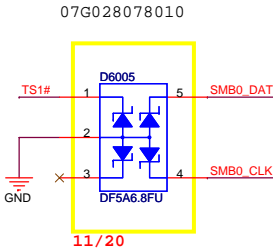
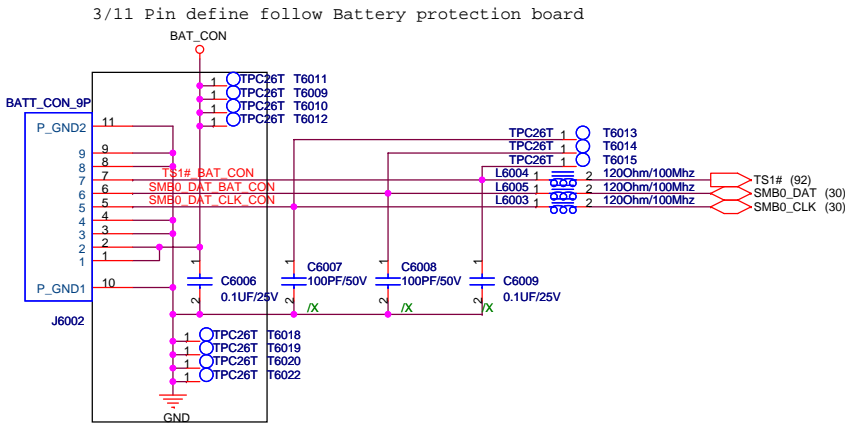


	5	4	3	2	1						
D					D						
C					C						
B					B						
A					A						
<div>ASUS®</div> <div>Title : BLANK</div> <div>ASUSTeK COMPUTER INC</div> <div>Engineer:</div> <table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>K40AA</td><td>1.00</td></tr></table> <div>Date: Wednesday, April 08, 2009</div> <div>Sheet 59 of 94</div>						Size	Project Name	Rev	A	K40AA	1.00
Size	Project Name	Rev									
A	K40AA	1.00									
	5	4	3	2	1						

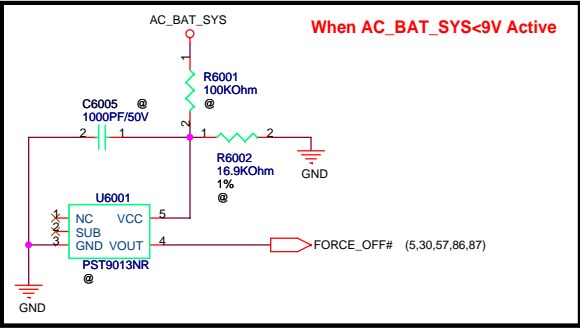
DC IN



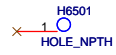
BAT IN



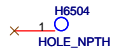
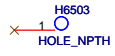
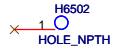
Without Battery & Pull out Adapter



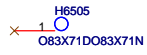
Hole-A



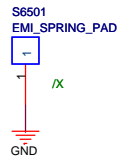
Hole-B



Hole-C

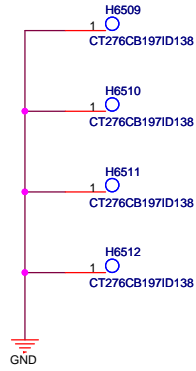


Spring

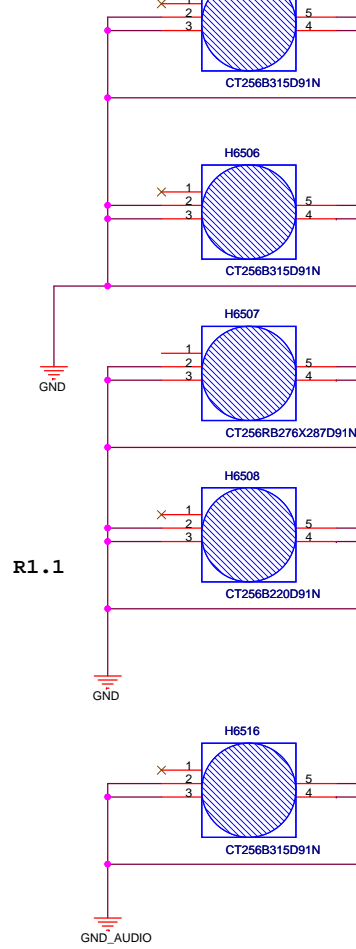


R1.2

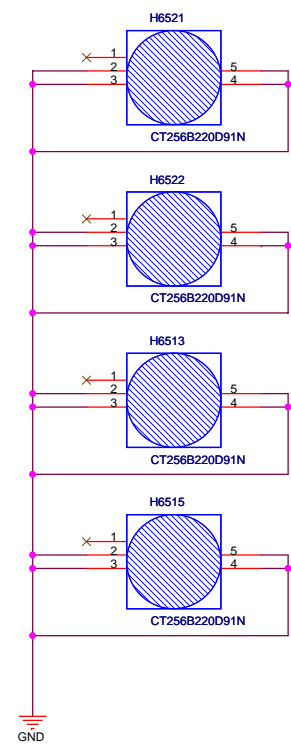
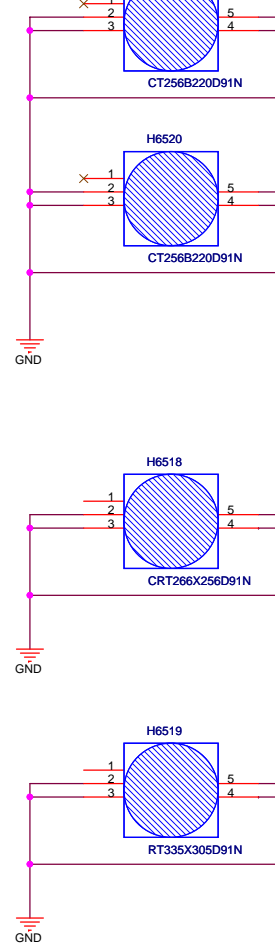
Hole-D

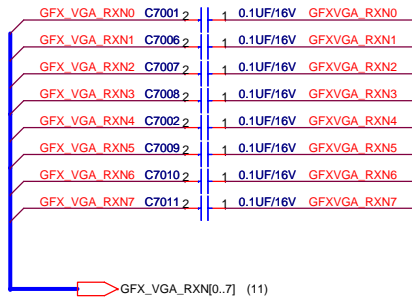


Hole-E

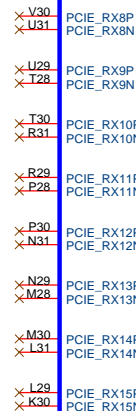
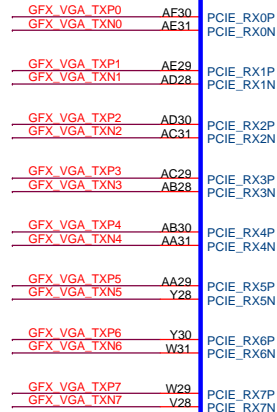


Hole-F

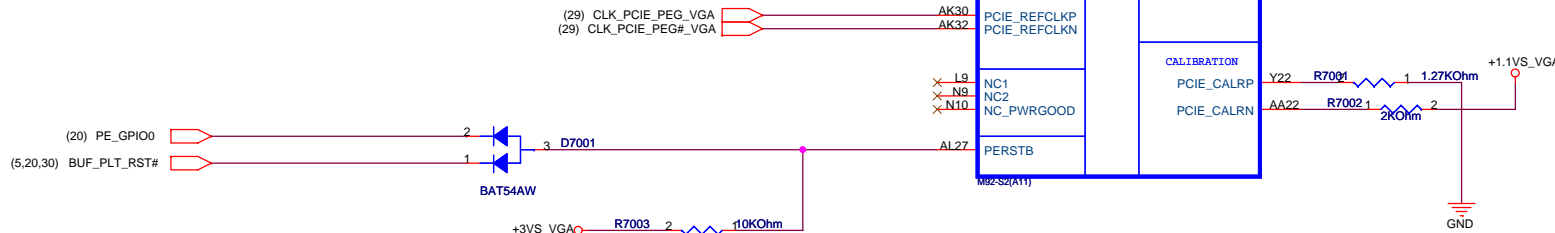
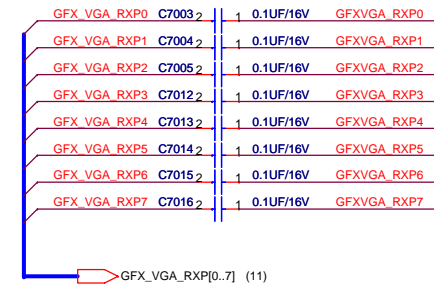
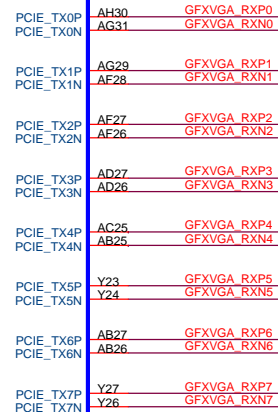




(11) GFX_VGA_TXP[0..7]
(11) GFX_VGA_TXN[0..7]



PCI EXPRESS INTERFACE

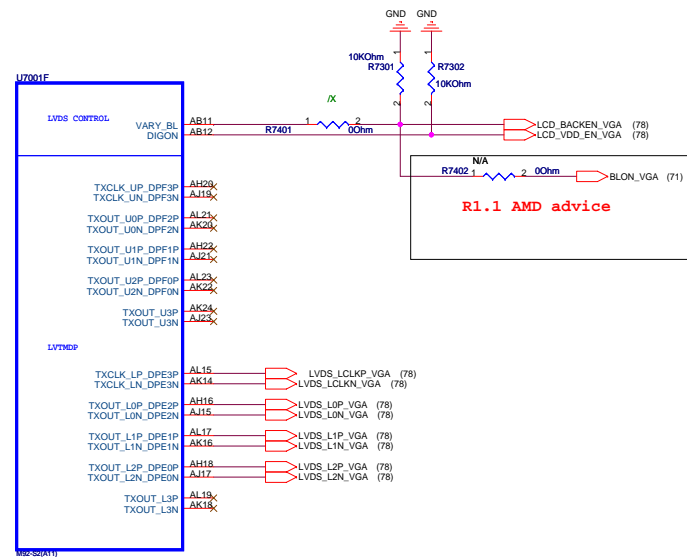


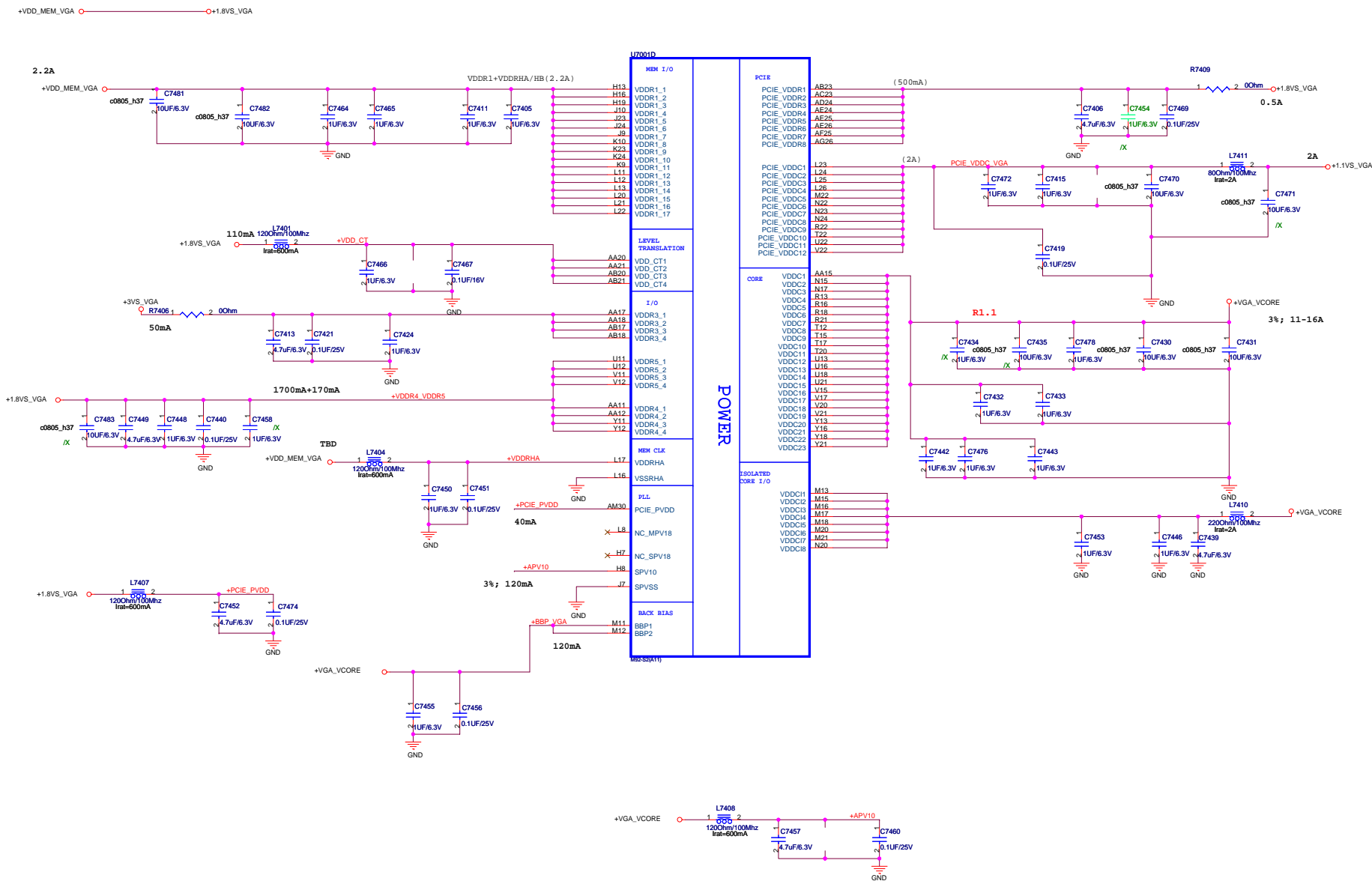
<Variant Name>

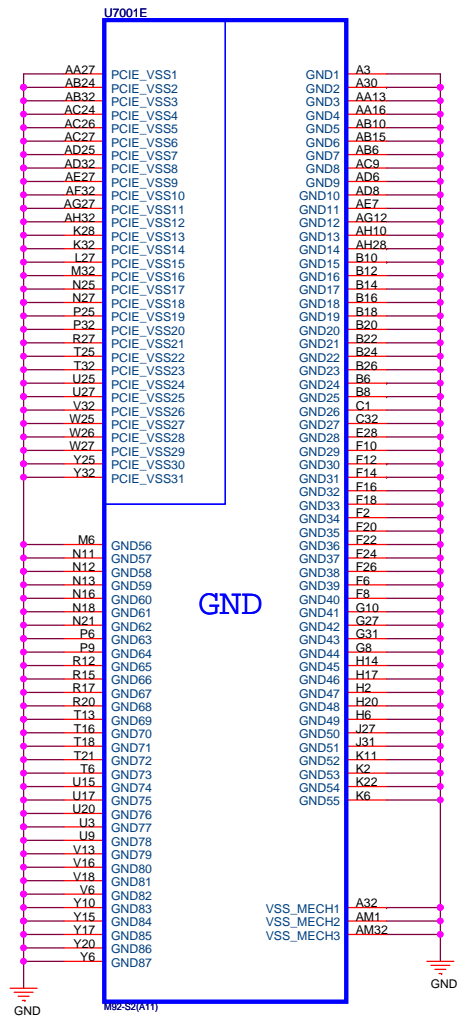
ASUS		Title : *	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	N11	1.0T	
Date: Wednesday, April 08, 2009		Sheet 70 of 94	

1.182V
1.082V
0.997V
0.925

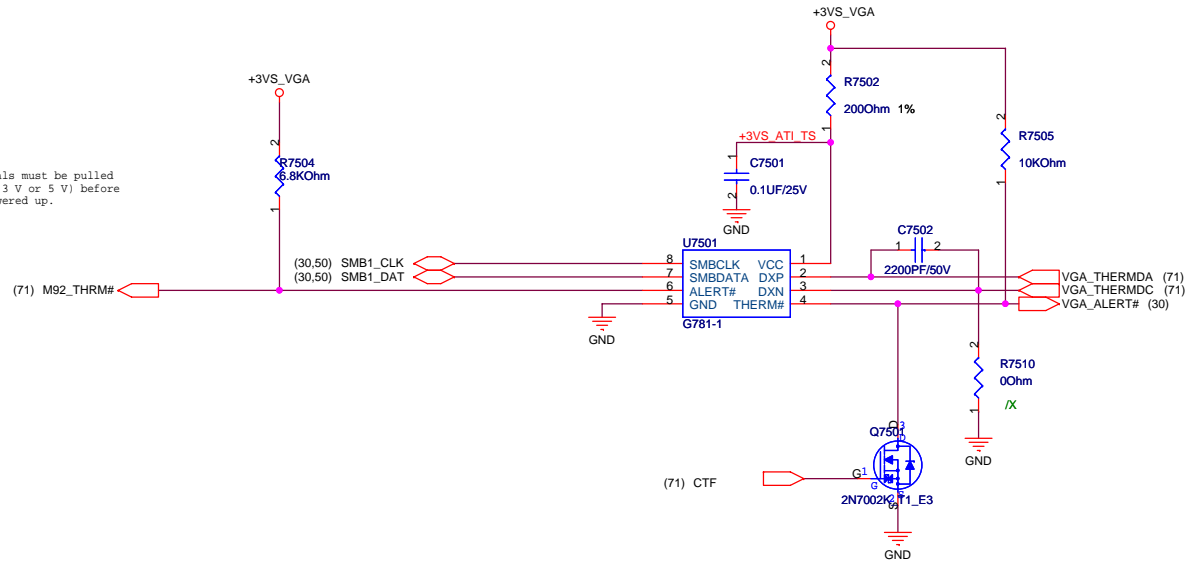




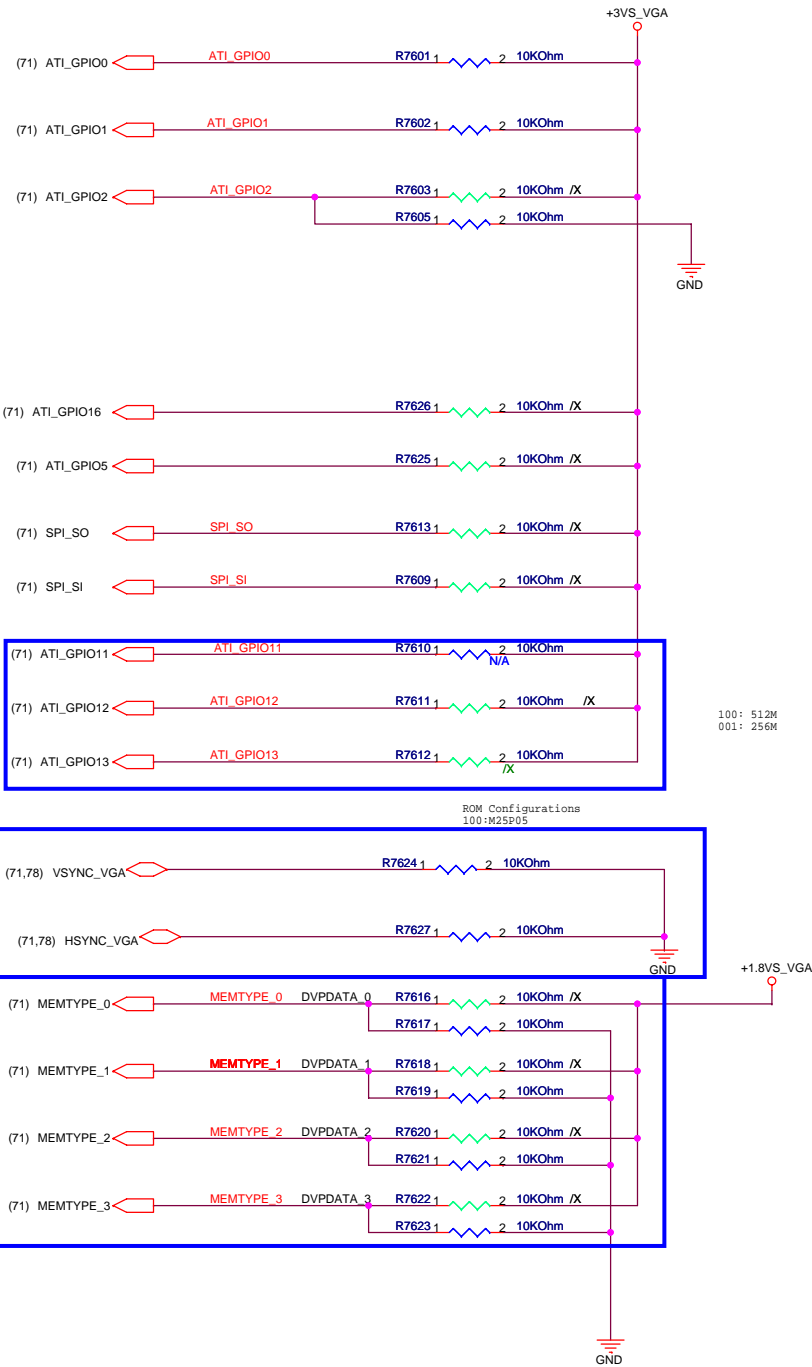




These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.



<Variant Name>



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO_1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO_2 - BIF_GEN2_EN (5.0 GT/s Enable)
0: Default (Driver Controlled Gen2)
1: Strap Controlled Gen2

GPIO(11,13,12) - CONFIG[2..0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)

CONFIG[2]
CONFIG[1]
CONFIG[0]

GPIO_8 - BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_5 - AMD BOARD FEATURES I
0: 1 RANK OF MEMORY 1: 2 RANKS OF MEMORY
BANK SELECT;

GPIO_16 - AMD BOARD FEATURES II
BANK SELECT;

GPIO_7 - TV OUT STANDARD
0 - PAL TVO
1 - NTSC TVO

V2SYNC - VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

GPIO_9 - VGA DISABLE : 1 for disable (set to 0 for normal operation)

HSYNC_VSYNC - AUD[1:0]
00 - No audio function
01 - Audio for DisplayPort and HDMI if adapter is detected
10 - Audio for DisplayPort only
11 - Audio for both DisplayPort and HDMI.

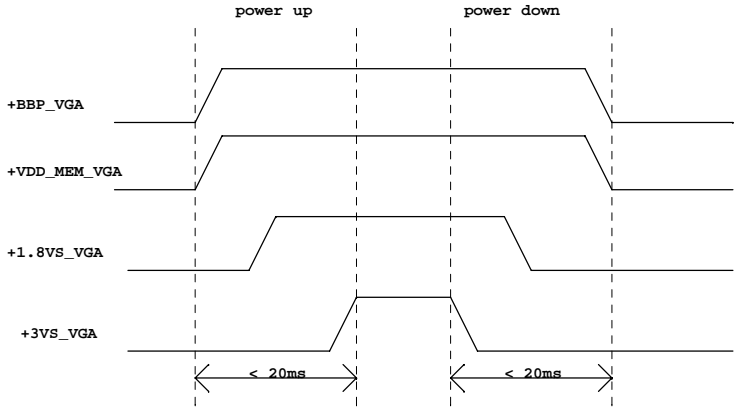
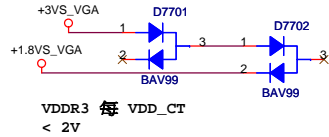
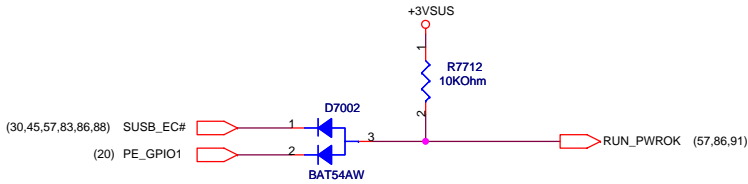
Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	64M*16	
Samsung	0001	1	64M*16	
Hynix				
Micron				

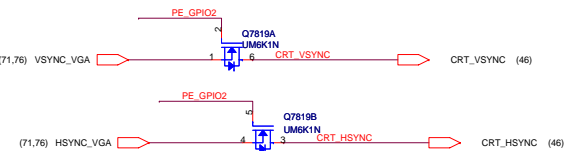
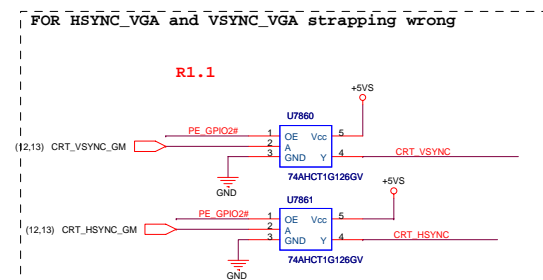
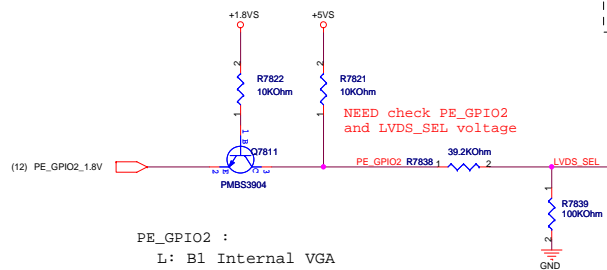
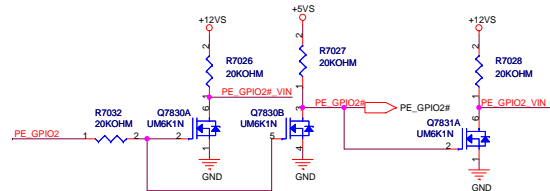
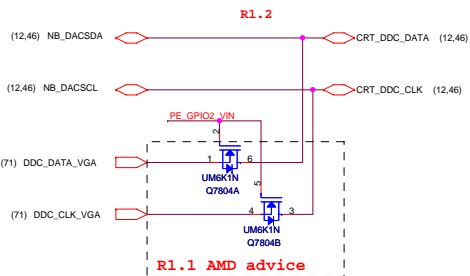
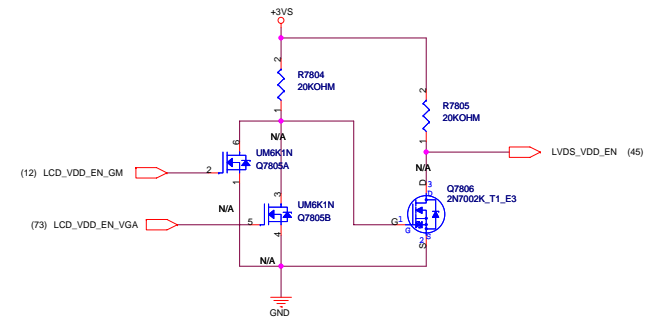
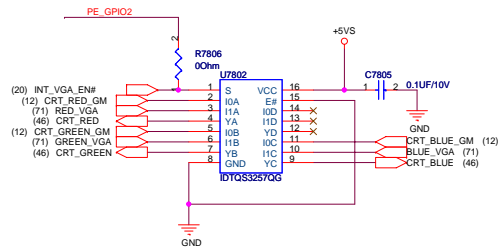
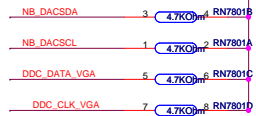
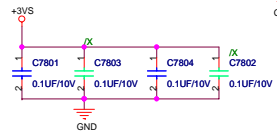
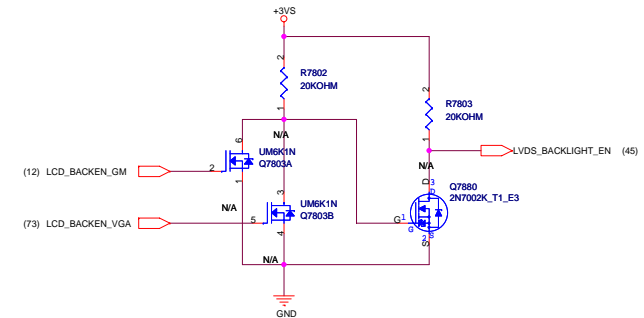
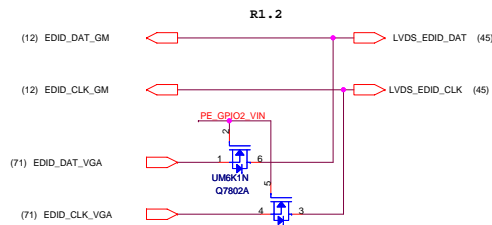
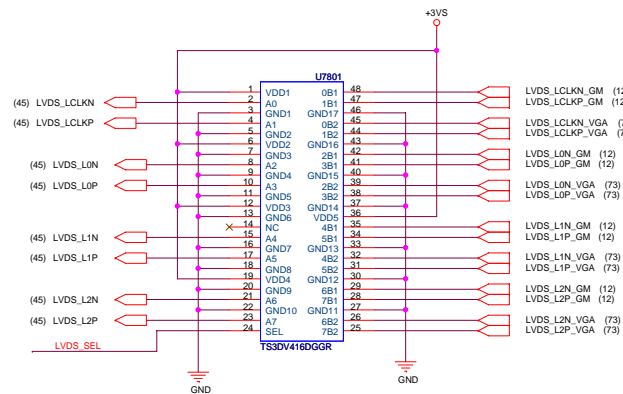
<Variant Name>

ASUS		Title : *	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	N11	1.0T	
Date:	Thursday, April 09, 2009	Sheet	76 of 94

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V



1.1-V rails should ramp before, or together with the 1.8-V rails.
The 1.1-V nominal voltage rails should never lag the 1.8-V nominal
voltage rails by more than 1.1 V within a 1 ms window.



POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET H: Enable

PE_GPIO1 MXM POWER ENABLE H: Enable

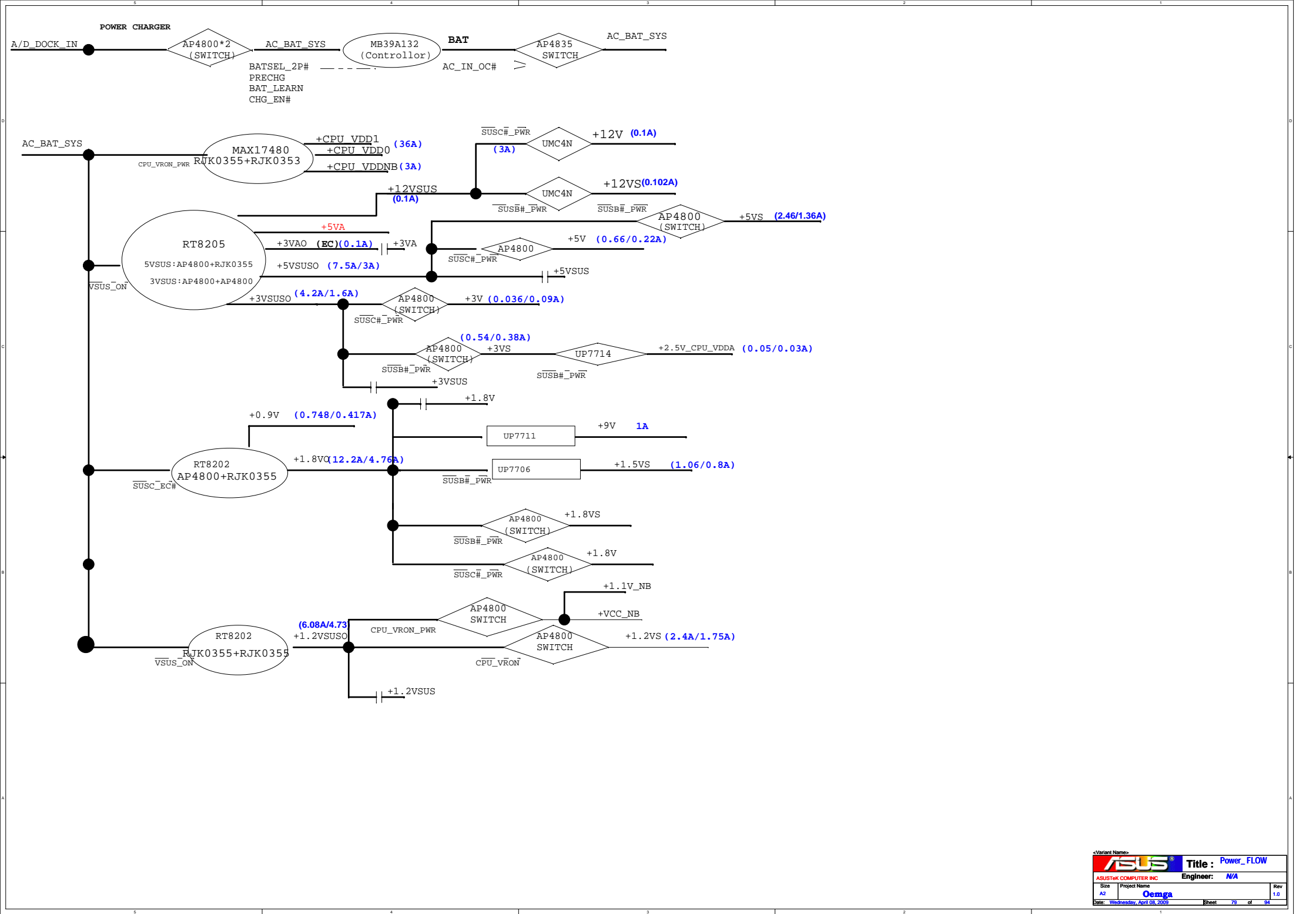
PE_GPIO2 MODE SWITCH

TMDS_HPD0 MXM HOT PLUG

PE_GPIO2 :

L: B1 Internal VGA

H: B2 External VGA



<Variant Name>



Title : Power_FLOW

ASUSTeK COMPUTER INC

Engineer: *N/A*

Size

A

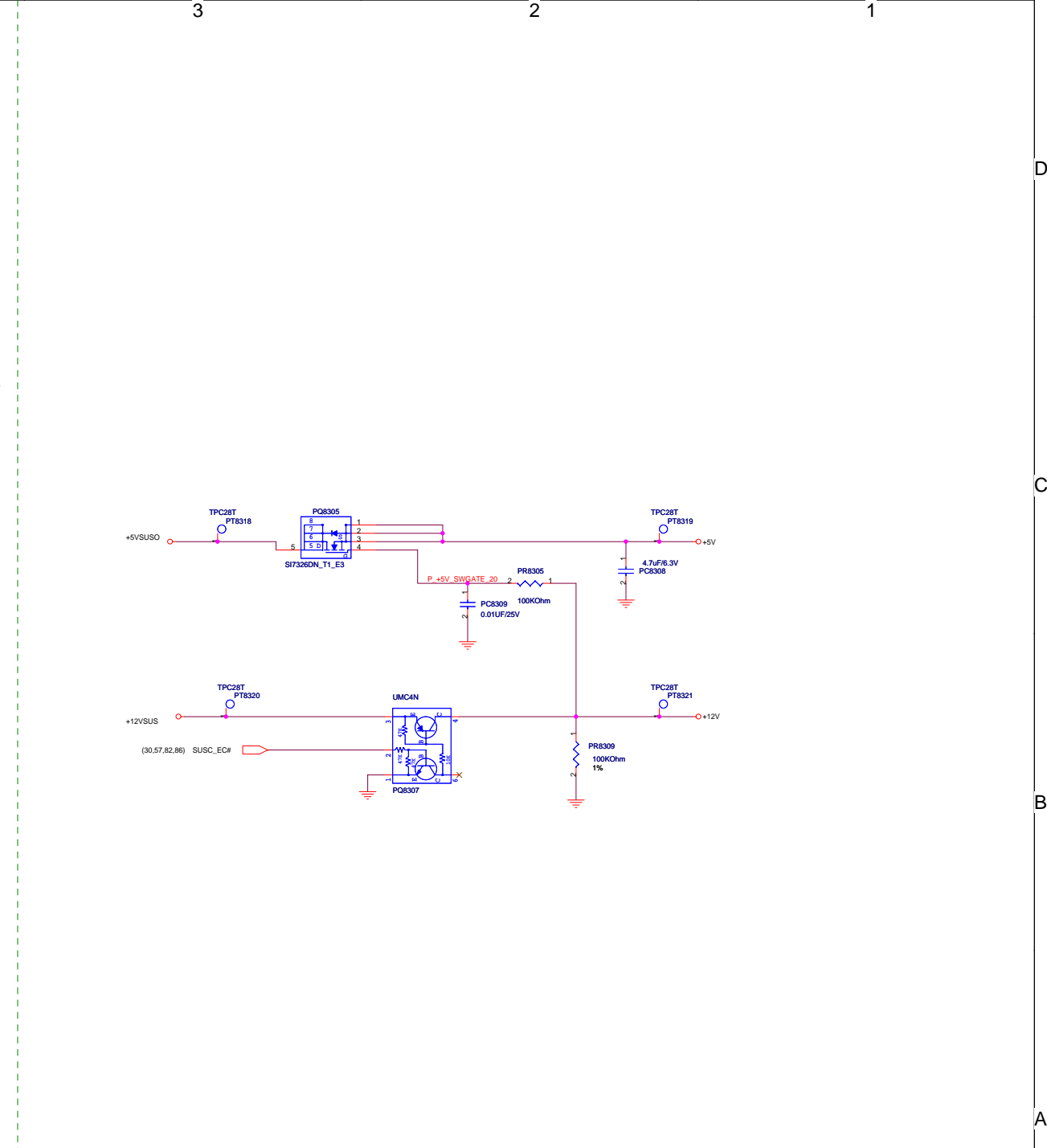
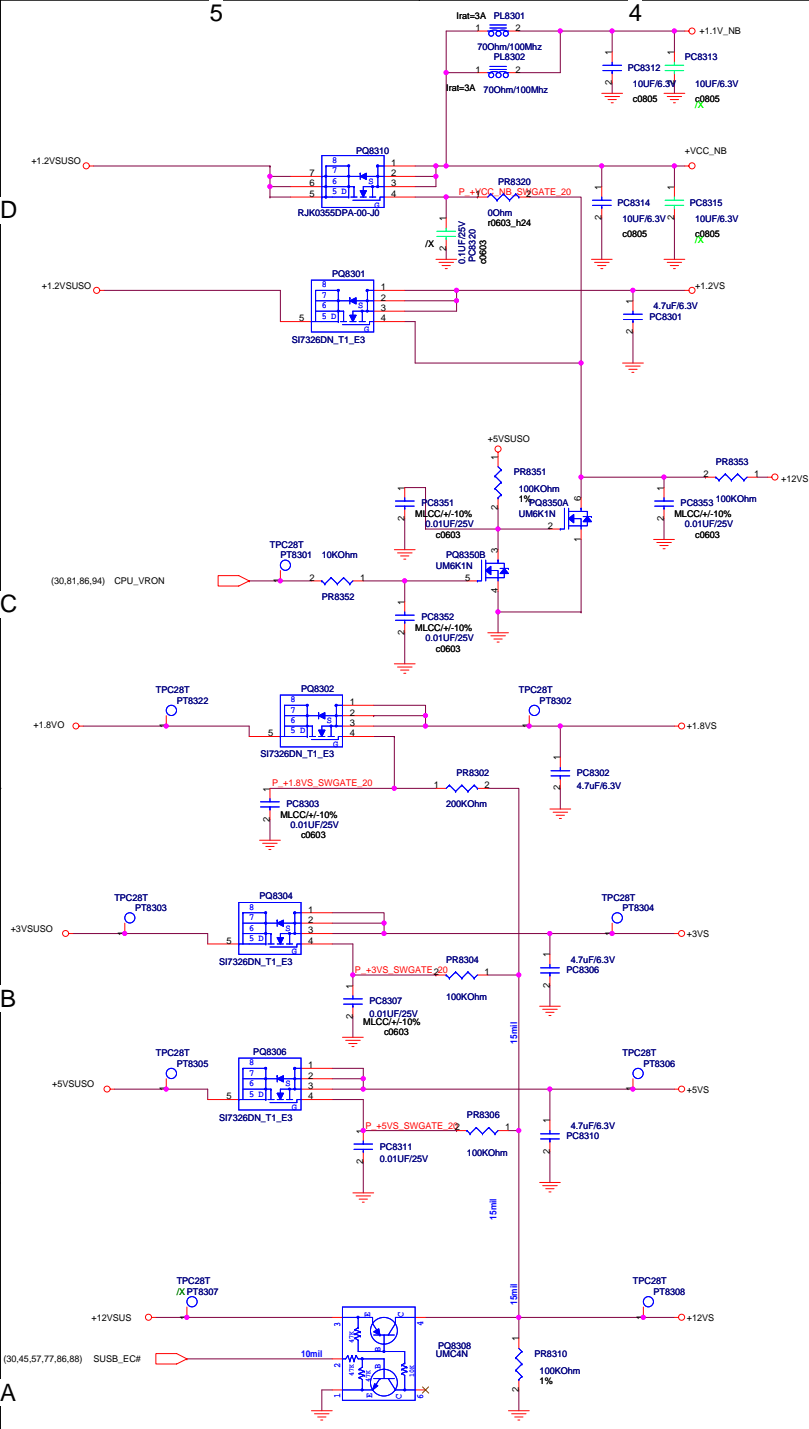
Project Name

Oemga

Rev
1.0


Date: Wednesday, April 08, 2009

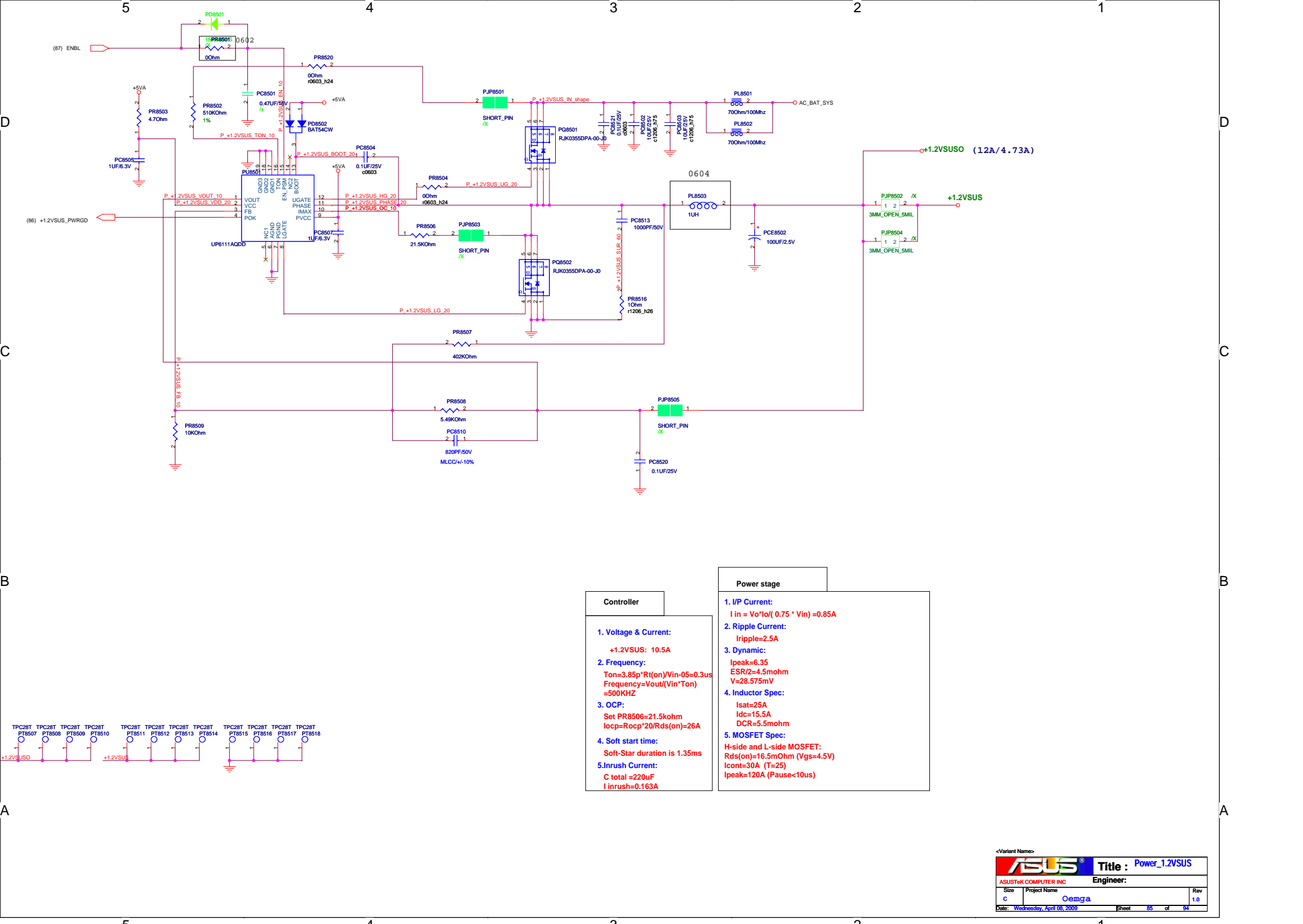
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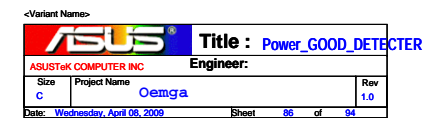


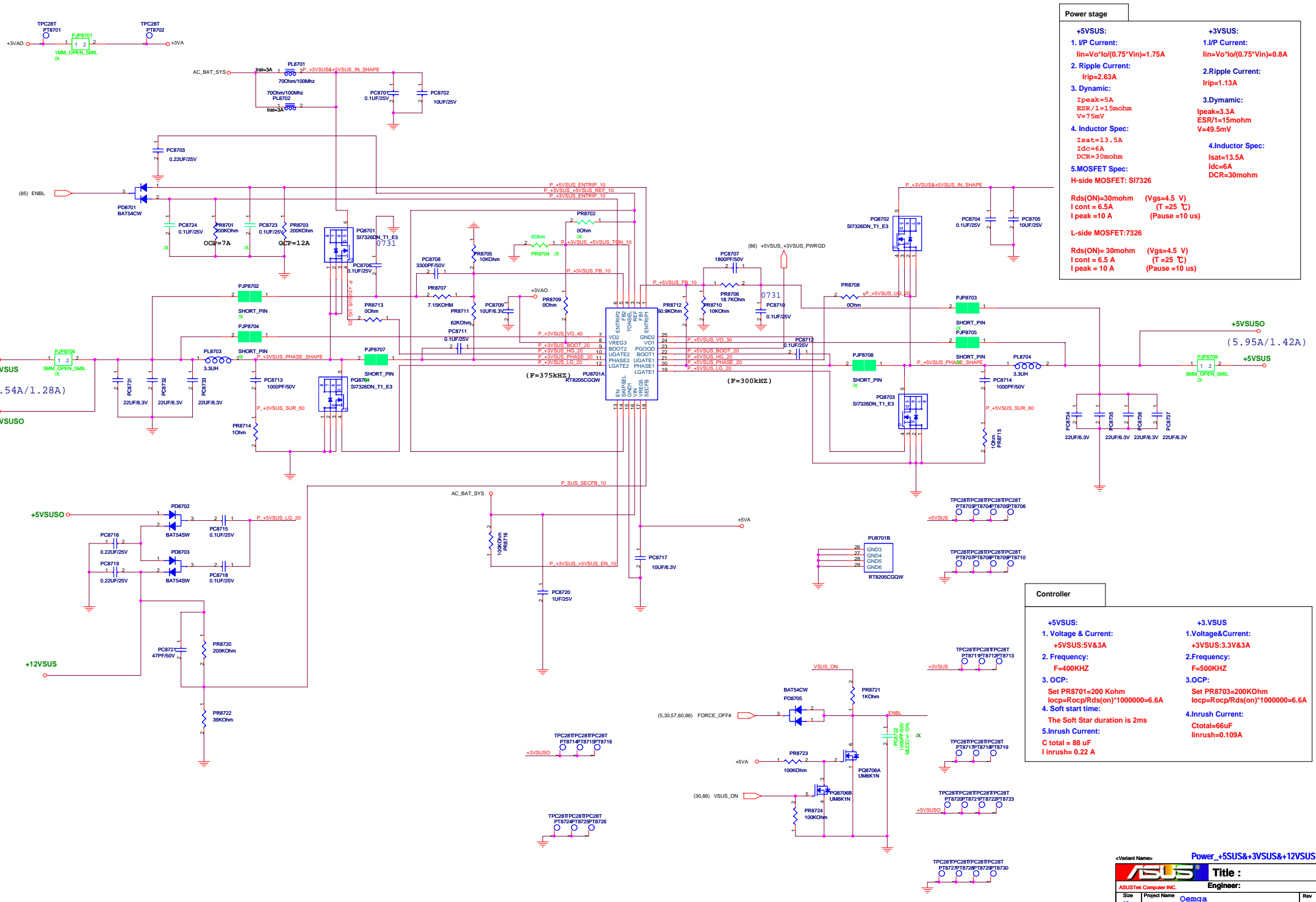
<Variant Name>

		Title : Power_Charger	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom			1.0
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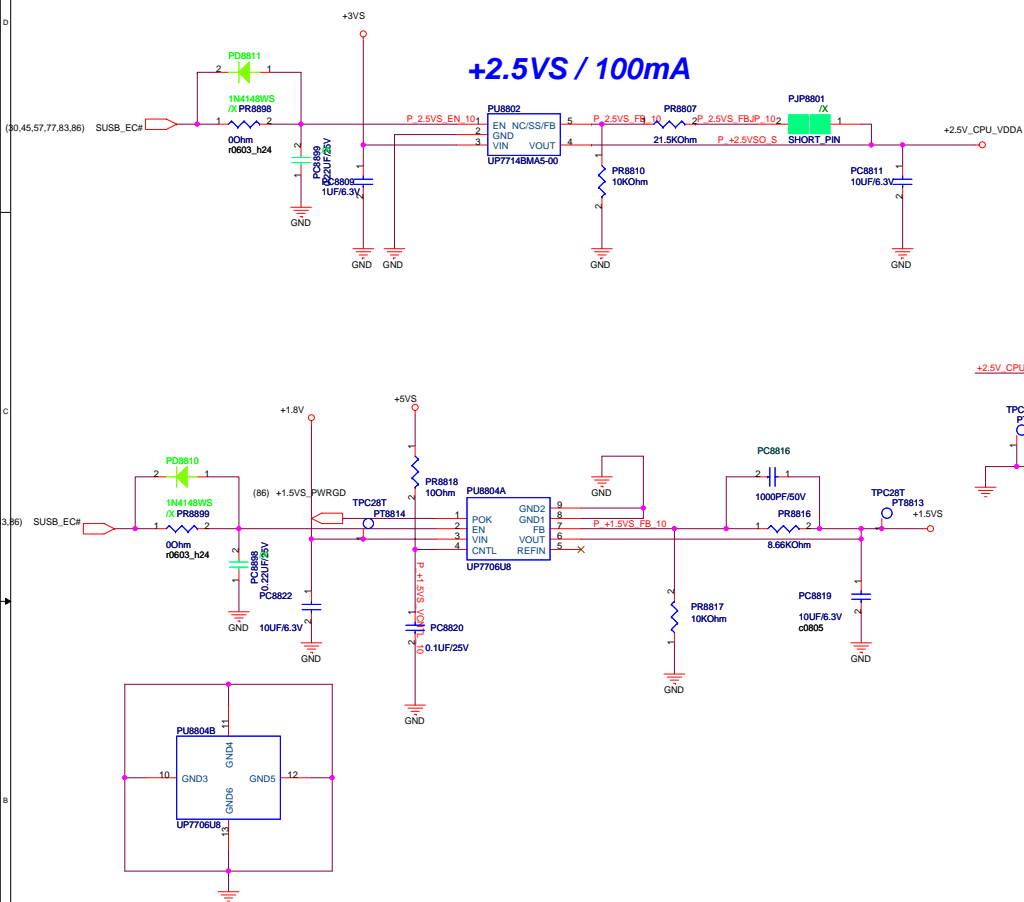
WWW.AliSaler.Com





Power stage	
+5VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.75A$ 2. Ripple Current: $I_{rip} = 2.63A$ 3. Dynamic: $I_{peak} = 5A$ $ESR / 1 = 1.5mohm$ $V = 75mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: SI7326 $R_{ds(ON)} = 30mohm$ $I_{cont} = 6.5A$ $I_{peak} = 10A$	+3VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.8A$ 2. Ripple Current: $I_{rip} = 1.13A$ 3. Dynamic: $I_{peak} = 3.3A$ $ESR / 1 = 15mohm$ $V = 49.5mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ L-side MOSFET: 7326 $R_{ds(ON)} = 30mohm$ $I_{cont} = 6.5A$ $I_{peak} = 10A$

Controller	
+5VSUS: 1. Voltage & Current: +5VSUS: 5V & 3A 2. Frequency: F = 400KHZ 3. OCP: Set PR8701 = 200 KOhm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Soft start time: The Soft Star duration is 2ms 5. Inrush Current: C total = 88 uF I inrush = 0.22 A	+3.VSUS 1. Voltage & Current: +3VSUS: 3.3V & 3A 2. Frequency: F = 500KHZ 3. OCP: Set PR8703 = 200KOhm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Inrush Current: Ctotal = 66uF Iinrush = 0.109A



2.5V @ 0.2A

1. Dropout Voltage:

$$\Delta V = 0.21V \text{ (} I_o = 0.3A \text{)}$$

2. Current Limit:

$$I_{\text{limit}} = 320mA$$

3. Continue Current:

$$I_{\text{cont}} = 300mA$$

4. Power Dissipation:

$$R_{\theta jc} = 250^{\circ}C/W$$

$$P_d = 0.4W$$

5. EN Voltage:

$$V_{\text{rising}} = 2V$$

$$V_{\text{falling}} = 0.8V$$

6. Supply Voltage:

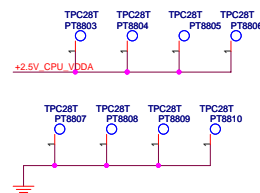
$$V_{cc} = 3V$$

7. Inrush current:

$$T_{ss} = 400\mu s$$

$$C_{\text{total}} = 10\mu F$$

$$I_{\text{inrush}} = 0.063A$$



+1.5VS @ 1.2A

1. Dropout Voltage:

$$\Delta V = 0.3V \text{ (} I_o = 2A \text{)}$$

2. Current Limit:

$$I_{\text{limit}} = 4A$$

3. Continue Current:

$$I_{\text{cont}} = 2A$$

4. Power Dissipation:

$$R_{\theta jc} = 52^{\circ}C/W$$

$$P_d = 1.9W$$

5. EN Voltage:

$$V_{\text{rising}} = 1.4V$$

$$V_{\text{falling}} = 0.8V$$

6. Supply Voltage:

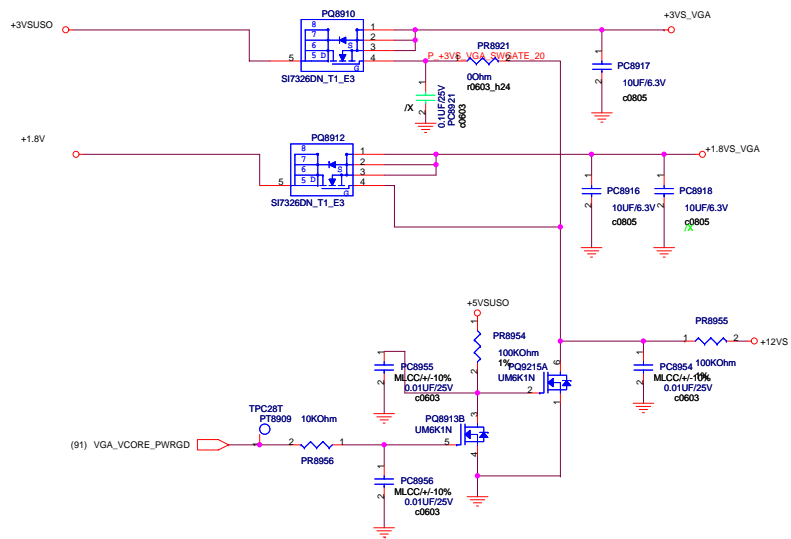
$$V_{cc} = 5V$$

7. Inrush current:

$$T_{ss} = 400\mu s$$

$$C_{\text{total}} = 10\mu F$$

$$I_{\text{inrush}} = 0.063A$$



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	1.02	-5%
0	1	1.071	Normal
1	0	1.12	+5%
1	1	1.171	+10%

Controller

1. Voltage & Current:
+1.2VSUS: 16A

2. Frequency:
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
~500KHZ

3. OCP:
Set PR8506=21.5kohm
Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:
Soft-Star duration is 1.35ms

5. Inrush Current:
C total =220uF
I inrush=0.163A

Power stage

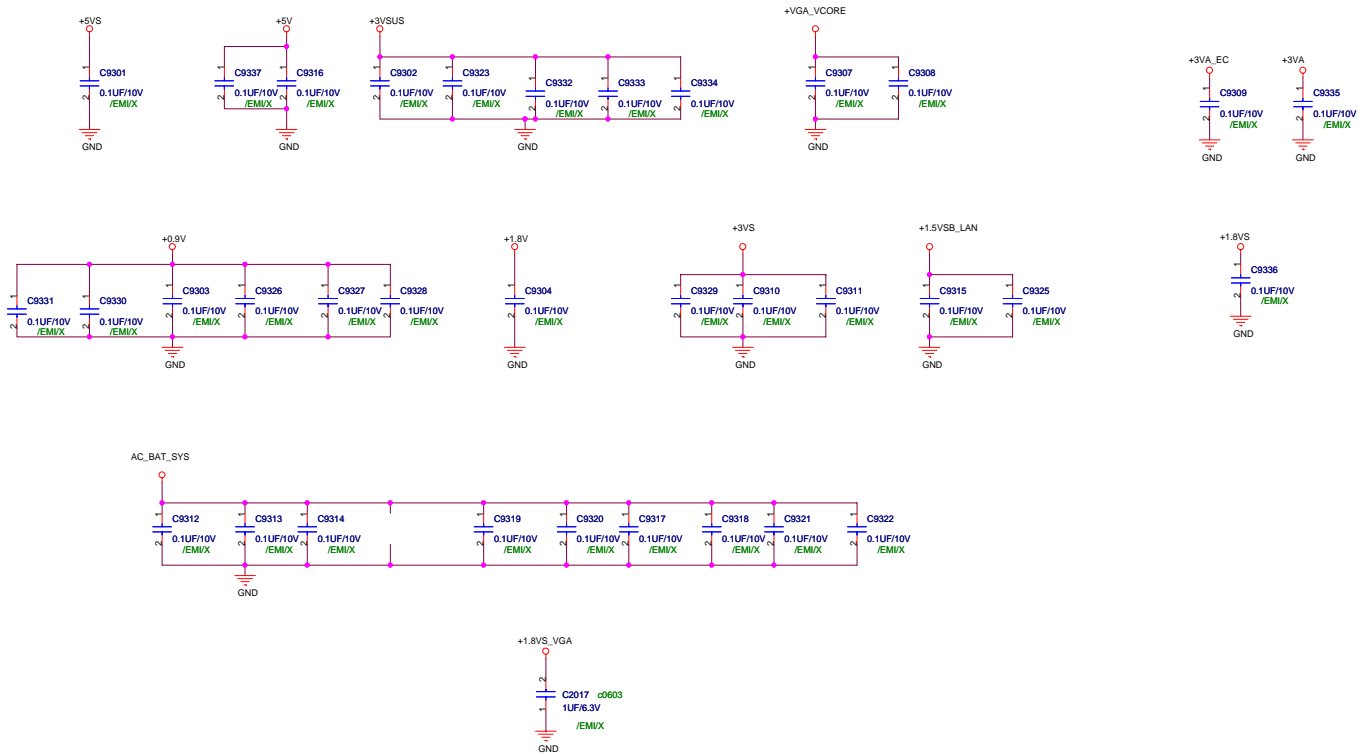
1. IP Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.85A$

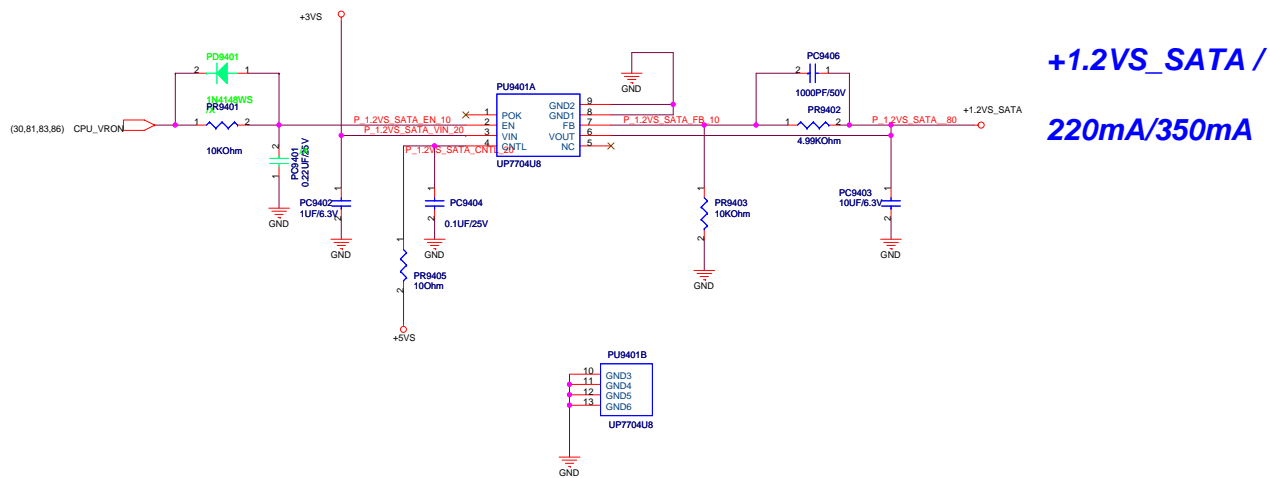
2. Ripple Current:
Iripple=3.74A

3. Dynamic:
Ipeak=6.1A
ESR/2=4.5mohm
V=27.5mohm

4. Inductor Spec:
Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)





**+1.2VS_SATA /
220mA/350mA**

- 1.2V @ 0.1A**
1. Dropout Voltage:
 $\Delta V = 0.3V$ ($I_o \approx 2A$)
 2. Current Limit:
 $I_{limit} \approx 2.5A$
 3. Continue Current:
 $I_{cont} = 2A$
 4. Power Dissipation:
 $R_{thjc} = 52^{\circ}C/W$
 $P_d = 1.8W$
 5. EN Voltage:
 $V_{rising} = 2V$
 $V_{falling} = 0.8V$
 6. Supply Voltage:
 $V_{cc} \approx 3V$
 7. Inrush current:
 $T_{ss} = 400\mu s$
 $C_{total} = 10\mu F$
 $I_{inrush} = 0.063A$